

# **Vehicle Computing**

Rugged Platforms for Vehicles and Railway Computing

# R6S User Manual

Version: 1.6 Date of Release: 2022-05-04

# **About this Document**

This manual describes the overview of the various functionalities of this product, and the information you need to get it ready for operation. It is intended for those who are:

- responsible for installing, administering and troubleshooting this system or Information Technology professionals.
- assumed to be qualified in the servicing of computer equipment, such as professional system integrators, or service personnel and technicians.

### **Icon Descriptions**

The icons are used in the manual to serve as an indication of interest topics or important messages. Below is a description of these icons:



**Note or Information**: This mark indicates that there is a note of interest and is something that you should pay special attention to while using the product.

**Warning or Important**: This mark indicates that there is a caution or warning and it is something that could damage your property or product.

# **Online Resources and Technical Support**

To obtain additional documentation resources and software updates for your system, please visit the <u>Lanner</u> <u>Download Center</u>. For certain categories of documents, please register for a Lanner Account at <u>Lanner's official</u> <u>website</u>, in order to access published documents and downloadable resources.

In addition to contacting your distributor or sales representative, you could visit our <u>Lanner Technical Support</u>, to fill in a support ticket to our technical support department.

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Your feedback is valuable to us, as it will help us continue to provide you with more accurate and relevant documentation. To provide any feedback, comments or to report an error, please email to <a href="mailto:contact@lannerinc.com">contact@lannerinc.com</a>. Thank you for your time.

### **Contact Information**

### **Taiwan Corporate Headquarters**

Lanner Electronics Inc. 7F, No.173, Sec.2, Datong Rd. Xizhi District, New Taipei City 22184, Taiwan 立端科技股份有限公司 221 新北市汐止區 大同路二段 173 號 7 樓 T: +886-2-8692-6060 F: +886-2-8692-6101 E: contact@lannerinc.com

### China

Beijing L&S Lancom Platform Tech. Co., Ltd. Guodong LOFT 9 Layer No. 9 Huinan Road, Huilongguan Town, Changping District, Beijing 102208 China T: +86 010-82795600 F: +86 010-62963250 E: <u>service@ls-china.com.cn</u>

### Canada

Lanner Electronics Canada Ltd 3160A Orlando Drive Mississauga, ON L4V 1R5 Canada T: +1 877-813-2132 F: +1 905-362-2369 E: sales ca@lannerinc.com

### USA

Lanner Electronics Inc. 47790 Westinghouse Drive Fremont, CA 94539 T: +1-855-852-6637 F: +1-510-979-0689 E: <u>sales us@lannerinc.com</u>

### **Europe**

Lanner Europe B.V. Wilhelmina van Pruisenweg 104 2595 AN The Hague The Netherlands T: +31 70 701 3256 E: <u>sales eu@lannerinc.com</u>

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# **Federal Communication Commission Interference Statement**

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by

turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- ▶ Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

### **FCC Caution**

- Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
- ► This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

# Note

1. An unshielded-type power cord is required in order to meet FCC emission limits and also to prevent interference to the nearby radio and television reception. It is essential that only the supplied power cord be used.

- 2. Use only shielded cables to connect I/O devices to this equipment.
- 3. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

### 🗥 Important

- 1. Operations in the 5.15-5.25GHz band are restricted to indoor usage only.
- 2. This device meets all the other requirements specified in Part 15E, Section 15.407 of the FCC Rules.

# **Safety Guidelines**

Follow these guidelines to ensure general safety:

- ▶ Keep the chassis area clear and dust-free during and after installation.
- Do not wear loose clothing or jewelry that could get caught in the chassis. Fasten your tie or scarf and roll up your sleeves.
- Wear safety glasses if you are working under any conditions that might be hazardous to your eyes.
- Do not perform any action that creates a potential hazard to people or makes the equipment unsafe.
- Disconnect all power by turning off the power and unplugging the power cord before installing or removing a chassis or working near power supplies
- > Do not work alone if potentially hazardous conditions exist.
- ▶ Never assume that power is disconnected from a circuit; always check the circuit.

# Consignes de sécurité

Suivez ces consignes pour assurer la sécurité générale :

- Laissez la zone du châssis propre et sans poussière pendant et après l'installation.
- Ne portez pas de vêtements amples ou de bijoux qui pourraient être pris dans le châssis. Attachez votre cravate ou écharpe et remontez vos manches.
- Portez des lunettes de sécurité pour protéger vos yeux.
- ▶ N'effectuez aucune action qui pourrait créer un danger pour d'autres ou rendre l'équipement dangereux.
- Coupez complètement l'alimentation en éteignant l'alimentation et en débranchant le cordon d'alimentation avant d'installer ou de retirer un châssis ou de travailler à proximité de sources d'alimentation.
- Ne travaillez pas seul si des conditions dangereuses sont présentes.
- ▶ Ne considérez jamais que l'alimentation est coupée d'un circuit, vérifiez toujours le circuit. Cet appareil génère, utilise et émet une énergie radiofréquence et, s'il n'est pas installé et utilisé conformément aux instructions des fournisseurs de composants sans fil, il risque de provoquer des interférences dans les communications radio.

# **Lithium Battery Caution**

- There is risk of Explosion if Battery is replaced by an incorrect type.
- Dispose of used batteries according to the instructions.
- Installation only by a skilled person who knows all Installation and Device Specifications which are to be applied.
- Do not carry the handle of power supplies when moving to another place.
- ▶ Please conform to your local laws and regulations regarding safe disposal of lithium BATTERY.
- Disposal of a battery into fire or a hot oven, or mechanically crushing or cutting of a battery can result in an explosion.
- Leaving a battery in an extremely high temperature surrounding environment can result in an explosion or the leakage of flammable liquid or gas.
- A battery subjected to extremely low air pressure that may result in an explosion or the leakage of flammable liquid or gas.

# Avertissement concernant la pile au lithium

- Risque d'explosion si la pile est remplacée par une autre d'un mauvais type.
- Jetez les piles usagées conformément aux instructions.
- L'installation doit être effectuée par un électricien formé ou une personne formée à l'électricité connaissant toutes les spécifications d'installation et d'appareil du produit.
- ▶ Ne transportez pas l'unité en la tenant par le câble d'alimentation lorsque vous déplacez l'appareil.

# **Operating Safety**

- Electrical equipment generates heat. Ambient air temperature may not be adequate to cool equipment to acceptable operating temperatures without adequate circulation. Be sure that the room in which you choose to operate your system has adequate air circulation.
- Ensure that the chassis cover is secure. The chassis design allows cooling air to circulate effectively. An open chassis permits air leaks, which may interrupt and redirect the flow of cooling air from internal components.
- Electrostatic discharge (ESD) can damage equipment and impair electrical circuitry. ESD damage occurs when electronic components are improperly handled and can result in complete or intermittent failures. Be sure to follow ESD-prevention procedures when removing and replacing components to avoid these problems.
- Wear an ESD-preventive wrist strap, ensuring that it makes good skin contact. If no wrist strap is available, ground yourself by touching the metal part of the chassis.
- Periodically check the resistance value of the antistatic strap, which should be between 1 and 10 megohms (Mohms).

### Sécurité de fonctionnement

- L'équipement électrique génère de la chaleur. La température ambiante peut ne pas être adéquate pour refroidir l'équipement à une température de fonctionnement acceptable sans circulation adaptée. Vérifiez que votre site propose une circulation d'air adéquate.
- Vérifiez que le couvercle du châssis est bien fixé. La conception du châssis permet à l'air de refroidissement de bien circuler. Un châssis ouvert laisse l'air s'échapper, ce qui peut interrompre et rediriger le flux d'air frais destiné aux composants internes.
- Les décharges électrostatiques (ESD) peuvent endommager l'équipement et gêner les circuits électriques. Des dégâts d'ESD surviennent lorsque des composants électroniques sont mal manipulés et peuvent causer des pannes totales ou intermittentes. Suivez les procédures de prévention d'ESD lors du retrait et du remplacement de composants.
- Portez un bracelet anti-ESD et veillez à ce qu'il soit bien au contact de la peau. Si aucun bracelet n'est disponible, reliez votre corps à la terre en touchant la partie métallique du châssis.
- Vérifiez régulièrement la valeur de résistance du bracelet antistatique, qui doit être comprise entre 1 et 10 mégohms (Mohms).

### **Mounting Installation Precaution**

The following should be put into consideration for rackmount or similar mounting installations:

- > Do not install and/or operate this unit in any place that flammable objects are stored or used in.
- The installation of this product must be performed by trained specialists; otherwise, a non-specialist might create the risk of the system's falling to the ground or other damages.
- Lanner Electronics Inc. shall not be held liable for any losses resulting from insufficient strength for supporting the system or use of inappropriate installation components.
- Elevated Operating Ambient If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient. Therefore, consideration should be given to installing the equipment in an environment compatible with the maximum ambient temperature (Tma) specified by the manufacturer.
- Reduced Air Flow Installation of the equipment in a rack should be such that the amount of airflow required for safe operation of the equipment is not compromised.
- Mechanical Loading Mounting of the equipment in the rack should be such that a hazardous condition is not achieved due to uneven mechanical loading.
- Circuit Overloading Consideration should be given to the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Appropriate consideration of equipment nameplate ratings should be used when addressing this concern.

 Reliable Grounding - Reliable grounding of rack mounted equipment should be maintained. Particular attention should be given to supply connections other than direct connections to the branch circuit (e.g. use of power strips).

### Installation & Operation :

This equipment must be grounded. The power cord for product should be connected to a socket-outlet with earthing connection.

Cet équipement doit être mis à la terre. La fiche d'alimentation doit être connectée à une prise de terre correctement câblée

 Suitable for installation in Information Technology Rooms in accordance with Article 645 of the National Electrical Code and NFPA 75.

Peut être installé dans des salles de matériel de traitement de l'information conformément à l'article 645 du National Electrical Code et à la NFPA 75.

- The machine can only be used in a restricted access location and must be installed by a skilled person. Les matériels sont destinés à être installés dans des EMPLACEMENTS À ACCÈS RESTREINT.
- This product is intended to be supplied by a Listed Power Adapter or DC power source, rated 12-24Vdc, 17.5-8A minimum, Tma = 70°C, and the altitude of operation = 5000m.

### **Electrical Safety Instructions**

Before turning on the device, ground the grounding cable of the equipment. Proper grounding (grounding) is very important to protect the equipment against the harmful effects of external noise and to reduce the risk of electrocution in the event of a lightning strike. To uninstall the equipment, disconnect the ground wire after turning off the power. A ground wire is required and the part connecting the conductor must be greater than 4 mm2 or 10 AWG.

### Consignes de sécurité électrique

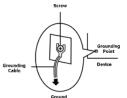
- Avant d'allumer l'appareil, reliez le câble de mise à la terre de l'équipement à la terre.
- Une bonne mise à la terre (connexion à la terre) est très importante pour protéger l'équipement contre les effets néfastes du bruit externe et réduire les risques d'électrocution en cas de foudre.
- > Pour désinstaller l'équipement, débranchez le câble de mise à la terre après avoir éteint l'appareil.
- Un câble de mise à la terre est requis et la zone reliant les sections du conducteur doit faire plus de 4 mm2 ou 10 AWG.

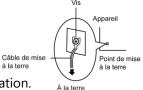
### **Grounding Procedure for Power Source**

- ▶ Loosen the screw of the earthing point.
- Connect the grounding cable to the ground.
- The protection device for the power source must provide 30 A current.
- ▶ This protection device must be connected to the power source before power.
- ▶ The cable hould 16 AWG

# Procédure de mise à la terre pour source d'alimentation

- Desserrez la vis du terminal de mise à la terre.
- Branchez le câble de mise à la terre à la terre.
- L'appareil de protection pour la source d'alimentation doit fournir 30 A de courant.
- Cet appareil de protection doit être branché à la source d'alimentation avant l'alimentation.
- Le câble doit 16 AWG





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# **CHAPTER 1 : PRODUCT OVERVIEW**

Built for rolling stock settings, R6S has gone through extensive vibration and shock testing. The system is certified with EN 50155, EN 50121-3-2, EN 50121-4, EN 50125-3 and EN 45545 standard as a fanless rolling stock computer. R6S not only features high-performance Intel Core i7-7600U CPU, but also boasts an abundance of I/O and internal expansion capabilities, including 10x M12 PoE ports, 1x Removable 2.5" drive bay for 2x storages, 2x COM ports, dual video ports (DVI-D/VGA), USB, and DIDO ports, making it perfect for rolling stock control and monitoring, infotainment, video surveillance and fleet management.

### **Main Features**

- Intel<sup>®</sup> Core i7-7600U Processor
- Certified with EN 50155, EN 50121-3-2, EN 50121-4, EN 50125-3 and EN45545 standard
- 10x rugged PoE ports with M12 connectors
- Support full size mini PCIe & M.2 sockets for LTE & Wi-Fi
- Wide range operating temperature from -40 to 70°C
- Onboard GPS receiver module and G-sensor
- 1x Removable 2.5" drive bay for 2x 2.5" storage (HDD/SSD is not included)
- Built-in CAN bus port
- Rich I/O: 2x USB 2.0, 2x USB 3.0, 2 x COM, DIO, Audio, VGA, DVI-D
- Built in wall mount kit

### **Package Content**

Your package contains the following items:

- 1x R6S Vehicle Computer
- 1x IR-RPB6SA1A DC to DC Adapter

# **Ordering Information**

SKU No.	Main Features
R6SA	Intel Core i7-7600U Processor, 2x miniPCIe socket with dual SIM, DC 32~96V power input
R6SB	Intel Core i7-7600U Processor, 1x miniPCIe socket, 4x M.2 with single SIM each, DC 24~36V power input
R6SC	Intel Core i7-7600U Processor, 1x miniPCIe socket, 4x M.2 with single SIM each, DC 72~110V power input

# System Specifications

	CPU	Intel® Core <sup>™</sup> i7-7600U CPU onboard
D	Frequency	2.8 GHz
Processor System	BIOS	AMI SPI Flash BIOS
	Chipset	SoC
Fanless		Yes
Tunicoo	Technology	1x DDR4 2133 SO-DIMM Socket
	Max. Capacity	Up to 16GB (Factory default: 16GB pre-installed)
Memory	Socket	1x 260-pin SODIMM
	Controller	4x Intel i210IT
	Speed	10/100/1000 Mbps
Ethernet	PoE	IEEE 802.3af
	Interface	M12 X-coded
Storage	Туре	1x Removable 2.5" drive bay for 2x storages (HDD/SSD not included)
Storage	LAN	1x GbE RJ45
	Display PoE	A SKU: 1x VGA, 1x resolution up to 2048x1536 DVI-D, resolution up to 1920x1200 B/C SKU: 2x HDMI, 1x resolution up to 3840x2160 10x IEEE 802.3af standard PoE ports
	Audio	Mic-in and Line-out with 2-watt by HD Audio
	Serial I/O	R6SA: RS-232/422/485 x2 with RI/5V/12V R6SB/C: RS-232/422/485 x4 with RI/5V/12V u-blox NEO-M8N; 3 GNSS (GPS, Galileo, GLONASS, BeiDou), default @
I/O	GPS	GPS+, GLONASS dual band
	G-sensor	ADXL 345
	CAN Port	1x CAN Bus J1939 / J1708 (Optional)
	Digital I/O	7x DI 12V TTL selectable, 7x DO 24V TTL, Max. 100mA 2x IGN-DI of ignition control to MCU
	USB	A SKU: 3x USB 2.0 Type A, 2x USB 3.0 Type A B/C SKU: 2x USB 2.0 Type A, 2x USB 3.0 Type A
	Antenna	A SKU: SMA antenna hole x6 (includes GPS+GLONASS x1); B/C SKU: SMA antenna hole x12 (includes GPS+GLONASS x1)
Expansion Interface	PCIe/USB	A SKU: Full-size Mini-PCIe Socket x2 with dual SIM card readers on each; B/C SKU: Full-size Mini-PCIe Socket x1, M.2 x4 with SIM card readers on each
e 1	Processor	Passive CPU heatsink
Cooling	System	Fanless design with corrugated aluminum
	Connector	5-pin M12 K-coded (Ground, DC_IN, Ground, IGN, Chassis Ground)
Power	Input	A SKU: DC 32~96V level, ATX mode, ignition delay on/off control; B SKU: DC 24~36V level, ATX mode, ignition delay on/off control; C SKU: DC 72~110V level, ATX mode, ignition delay on/off control
	Output	A SKU: 12V/2A out; B/C SKU: N/A
	Hardware	Fintek F81866AD-I integrated watchdog timer
Miscellaneous	Internal RTC with Li Battery	Yes
	Operating Temp	-40~70°C / -40~158°F
Environment	Storage Temp	-40~85°C / -40~185°F
	Humidity	5%~95% @ 40°C / 104°F (Storage Level)
	Dimension (WxHxD)	272.4 x 121.3 x 228 mm (10.72" x 4.77" x 8.97")
Mechanical	Weight	8 kg
wechanica	Mounting	Wall mount kit
OS Support	Microsoft Windows	Win10 IoT Enterprise
OS Support	Linux	Redhat Enterprise 5, Fedora 14. Linux Kernel 2.6.18 or later
		10

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Certification	EMC	FCC/CE Class A, RoHS
	Safety	E-13 include ISO-7637-2
	( ARTITIAN	IP rated 50, MIL-STD-810G, EN 50155, EN 50121-3-2, EN 50121-4, EN 50125-3, and EN 45545

# Front Panel (R6SA/B/C)



No.		Description
F1	System Status LED Indicator	System Power Status System Status HDD Status
F2	USB 3.0 Port	2x USB 3.0 Type A
F3	USB 2.0 Port	2x USB 2.0 Type A
F4	GbE Port	1x RJ45 port with LED indicators
F5	SIM Cover	A SKU: 2x Dual SIM card socket B/C SKU: 5x Single SIM card socket
F6	Storage Lock	Lock for removable 2.5" storage caddy
F7	Antenna Port	LTE Antenna Wi-Fi Antenna
F8	Storage Bay	2x SATA interface storage bays to support removable 2.5" HDD/SSD drive
F9	SD Card	SD Card socket

# Rear Panel (R6SA)



No.	Description							
	2 3	10x M12X-coded 8-pin PoE Port						
	PoE Port 1	Pin	Signals	Pin	Signals			
R1	8005	1	LANx*_MX0P	2	LANx*_MX0N			
		3	LANx*_MX1P	4	LANx*_MX1N			
	/ 6	5	LANx*_MX3P	6	LANx*_MX3N			
		7	LANx*_MX2N	8	LANx*_MX2P			
		1x M12 K-coded 5-pin for power source, DC 32~96V level						
			, DC_IN, Ground, I					
	DC Input	Pin	Signals	Pin	Signals			
R2		1	GND	2	DC_VIN			
	PE	3	MCU_PG	4	IGN_IN			
		5(PE)	CHASSIS GND					
	3		A-coded 5-pin for		· ·			
R3	DC Output	<b>Pin</b> 1	Signals 12V_Output	<b>Pin</b> 2	Signals FORWARD			
ND ND		3	SPEED	4	12V GND			
	5	5	GPS GND		120_0100			
R4	DVI-D Port	1x DVI-I	D Connector					
R5	VGA Port	1x VGA	DB15 Connector					
		2x DB9 N	Male Connector for	r RS232,	/422/485			
		Pin	Signals	F	Pin Signals			
		1_down	COM1_C_DCD_TN		·			
	9 6	3_down	COM1_C_TXD_RP	4_u	ip COM1_C_DTR_RN			
	COM Port	5_down	GND_COM	6_u	IP COM1_C_DSR			
R6	5 1	7_down	COM1_C_RTS	8_u	ip COM1_C_CTS			
	- 1	9_down	COM1_C_RI					
		1_up	COM2_C_DCD_TN		down COM2_C_RXD_TF			
		3_up	COM2_C_TXD_RP	_	down COM2_C_DTR_RN			
		5_up 7_up	GND_COM COM2_C_RTS	-	lown COM2_C_DSR lown COM2_C-CTS			
		9_up	COM2_C_RI	0_0				

1		1x DB26 Female Connector for GPIO & CAN Bus						
l		Pin	Signals	Pin	Signals	Pin	Signals	
		1	CAN_H/J1939+_R	10	CAN_L/J1939R	19	DO_5	
	19 26	2	DI_0	11	DGIN_0	20	12V_GND	
		3	DI_1	12	J1850+/J1708+_R	21	12V_GND	
R7	Multi-IO	4	DI_2	13	J1850-/J1708-R	22	DO_0	
		5	DI_3	14	DO_6	23	DO_1	
		6	12V_GND	15	DGIN_1	24	DO_2	
		7	GND_CAN	16	DI_4	25	DO_3	
		8	V_CAR BAT	17	GND_CAN	26	DO_4	
		9	DI_COM	18	DI_6			
	9 6	L/R-ch Pin	annels via 9-pin fe Signals		connector. Pin Signals	S		
	Audio Port					GND AUD		
R8		1	MIC IN R					
	5 1	3	MIC_IN_R X			JD		
	5 1				2 GND_AU	ID ID	_	
	5 1	3	X		2 GND_AL 4 GND_AL	JD JD _L		
	5. 1	3	X AMPOUT_R		2 GND_AL 4 GND_AL 6 MIC_IN	JD JD _L		
R9	Antenna Port (GPS+GLONASS default)	3 5 7 9 1x 3 G	X AMPOUT_R GND_AUD AMPOUT_L	GLON	2 GND_AU 4 GND_AU 6 MIC_IN_ 8 GND_AU	ID ID L ID		
R9		3 5 7 9 1x 3 G (G-sen	X AMPOUT_R GND_AUD AMPOUT_L NSS (GPS, Galileo,	GLON	2 GND_AU 4 GND_AU 6 MIC_IN_ 8 GND_AU	ID ID L ID		
R9		3 5 7 9 1x 3 G (G-sen	X AMPOUT_R GND_AUD AMPOUT_L NSS (GPS, Galileo, isor no antenna ne	GLON eeded)	2 GND_AU 4 GND_AU 6 MIC_IN_ 8 GND_AU	JD JD L JD na,		
R9 R10		3 5 7 9 1x 3 G (G-sen 2x USE	X AMPOUT_R GND_AUD AMPOUT_L NSS (GPS, Galileo, sor no antenna ne 3 2.0 Type A	GLON eeded)	2 GND_AU 4 GND_AU 6 MIC_IN_ 8 GND_AU JASS, BeiDou) anteni	JD JD _L JD na, s		
	(GPS+GLONASS default)	3 5 7 9 1x 3 G (G-sen 2x USE Pin	X AMPOUT_R GND_AUD AMPOUT_L NSS (GPS, Galileo, sor no antenna ne 3 2.0 Type A Signals	GLON eeded)	2 GND_AU 4 GND_AU 6 MIC_IN_ 8 GND_AU JASS, BeiDou) anteni 9 Pin Signal	JD JD _L JD na, s		

# Rear Panel (R6SB/C)



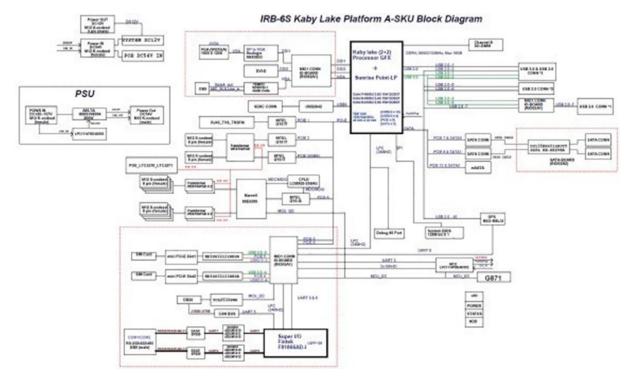
#### **Grounding Point:**

For safety measures to help prevent people from accidentally coming in contact with electrical hazards.

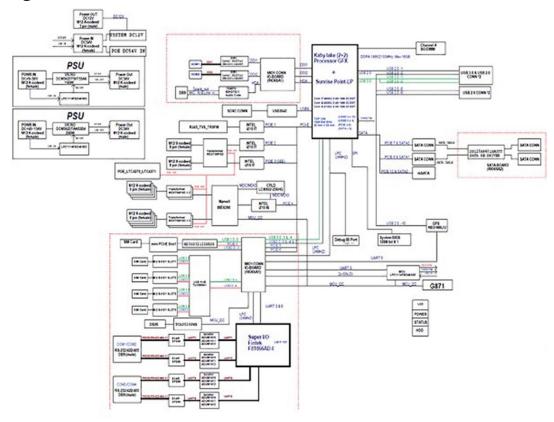
No.				Descri	ptior	ı	
		2 3	10x M1	2X-coded 8-pin PoE	Port		
	PoE Port		Pin	Signals	Pin		Signals
R1	TOLIOI	8 0 0 5	1	LANx*_MX0P	2		LANx*_MX0N
<b>N</b> 1		00	3	LANx*_MX1P	4		LANx*_MX1N
		7 6	5	LANx*_MX3P	6		LANx*_MX3N
			7	LANx*_MX2N	8		LANx*_MX2P
			1x M12	K-coded 5-pin for p	ower	sourc	ce, (Ground, DC_IN, G
			Ground	)			
	DC Input	3 • • 2	B SKU:	DC 24~36V level; C S	KU: [	DC 72	~110V level
R2	Demput		Pin	Signals	Pin		Signals
		PE	1	GND	2		DC_VIN
			3	MCU_PG	4		IGN_IN
			5(PE)	CHASSIS GND			
	COM 1 Port (	Console)		<i></i>	<b></b>		
		console)	Pin	Signals COM1_C_DCD_TN	Pin		Signals COM1_C_RXD_TP
20	9	6	1	COM1_C_DCD_TN COM1_C_TXD_RP	2	+	COM1_C_DTR_RN
R3	•	<b>.</b>	3	COMI_C_IAD_RP	4		COM1_C_DIR_RN
	5	1	5	COM1_2_GND	8	+	COM1_C_CTS
			9	COM1_C_RI	0	+	comi_c_ci5
			3		I		
	6014 B B		Pin	Signals		Pin	Signals
	COM 2 Port		1	COM2_C_DCD_TN		2	COM2_C_RXD_TP
<b>D</b> 4	9	6	3	COM2_C_TXD_RP	T	4	COM2_C_DTR_RN
R4	• 🔐	<b></b>	5	COM2_2_GND		6	COM2_C_DSR
	5	1	7	COM2_C_RTS		8	COM2_C_CTS
			9	COM2 C RI			

	COM 4 Port	Pin	Signals		Pin	Signals	
	9 6	1_up	COM4_C_DCD_TN			OM4_C_RXD_TP	
R5	·	3_up	COM4_C_TXD_RP	4	Lup CC	DM4_C_DTR_RN	
	5 1	5_up	COM4_2_GND			COM4_C_DSR	
		7_up	COM4_C_RTS	6	3_up	COM4_C_CTS	4
		9_up	COM4_C_RI				
	COM 5 Port	Pin	Signals	Pin	Si	gnals	
	20101 3 FOIL 9 6	1_up	COM5_C_DCD_TN	2_up	COM5_C_F	RXD_TP	
R6		3_up	COM5_C_TXD_RP	4_up	COM5_C_E		
NU		5_up	COM5_2_GND	6_up	COM5_C		
		7_up	COM5_C_RTS	8_up	COM5_C	_CTS	
		9_up	COM5_C_RI				
R7	Display Port	2x HDM	l Ports				
		1x DB26	Female Connector f	or GPIC	0 & CAN Bu	S	
		Pin	Signals	Pin	Sign	als Pin	Signals
	Multi-IO	1	FORWARD_CONN	10	SPEED_C	CONN 19	DO_5
		2	DI_0	11	DGIN	I_0 20	12V_GND
	9 6	3	DI_1	12	GND_	GPS 21	12V_GND
R8		4	DI_2	13	Х	22	DO_0
NO		5	DI_3	14	DO	6 23	DO_1
		6	DIO_GND	15	DGIN	L1 24	DO_2
		7	X	16	DL		DO_3
		8	Х	17	DI		DO 4
		9	DI_COMMON	18	 DI_	6	 DO_5
		1x Realte	ek ALC886-GR, supp	orts ext	ernal audio	I/O for Mic-in/L	ine-out with
			via 9-pin Female C			,	
	Audio Port	Pin	Signals	Pin	Signals		
	19 26	1	MIC_IN_R	2	GND_AUD		
R9		3	Х	4	GND_AUD		
	1 9	5	AMPOUT_R	6	MIC_IN_L		
		7	GND_AUD	8	GND_AUD		
		9	AMPOUT_L				
R10	Antenna Port	6x LTE A	ntenna Port				
R11	Antenna Port	IX 5 GIV.	55 (GPS, Gailleo, GLC	JINA33,	beiDou) an	tenna support	

# Motherboard Information Block Diagram (A SKU)

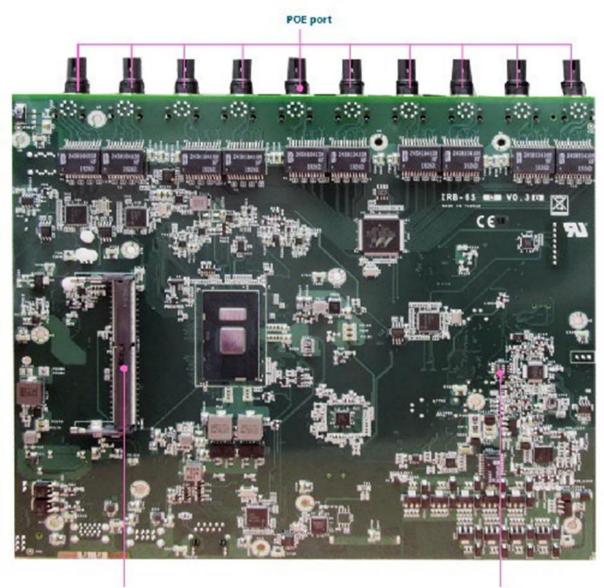


### Block Diagram (B/C SKU)



# **Motherboard Layout**

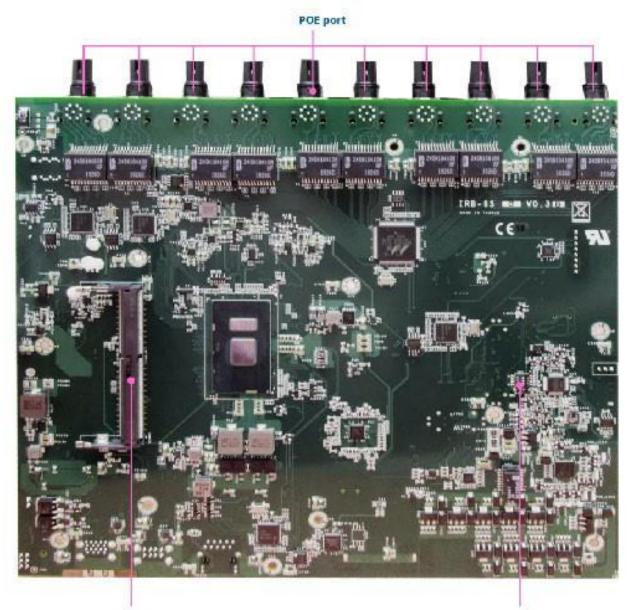
### **Front View**



DIMM1

SW1

### **Rear View**

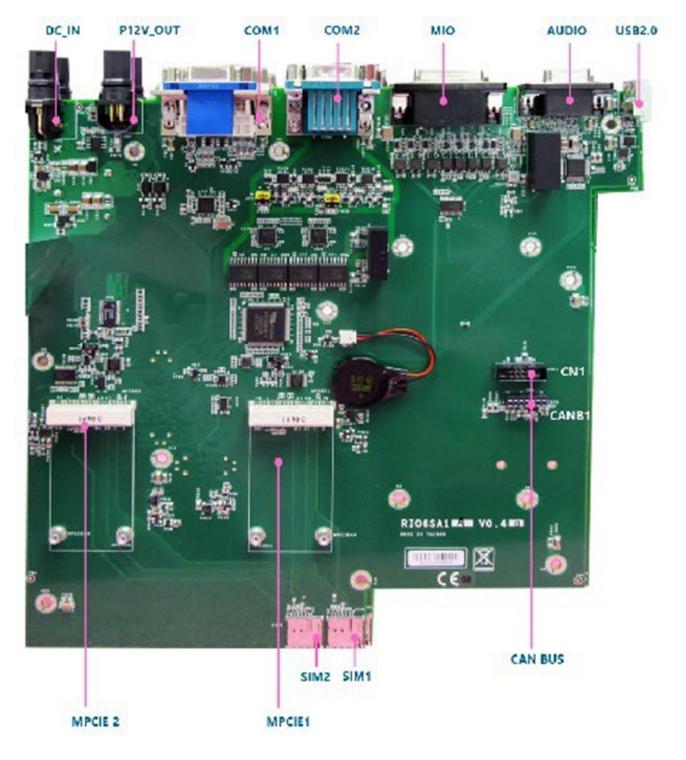


DIMM1

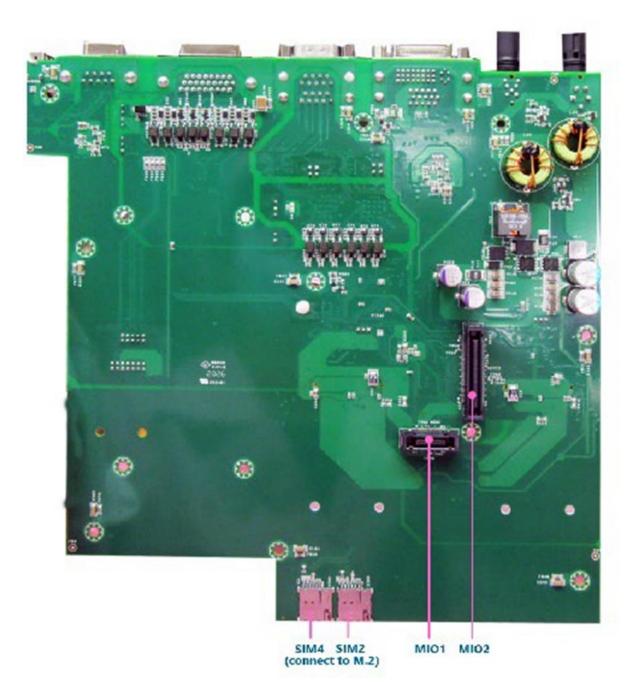
SW1

# IO Board Layout (A SKU)

**Front View** 

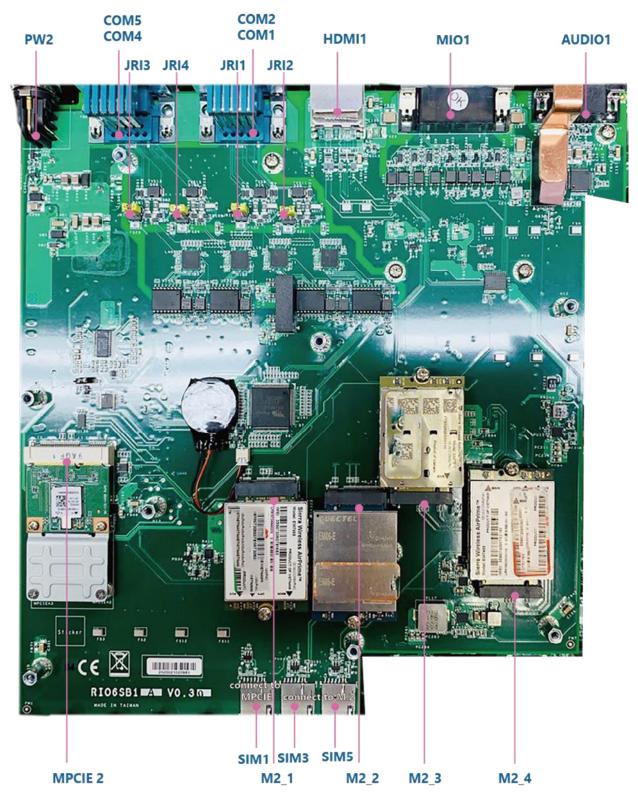


#### **Rear View**

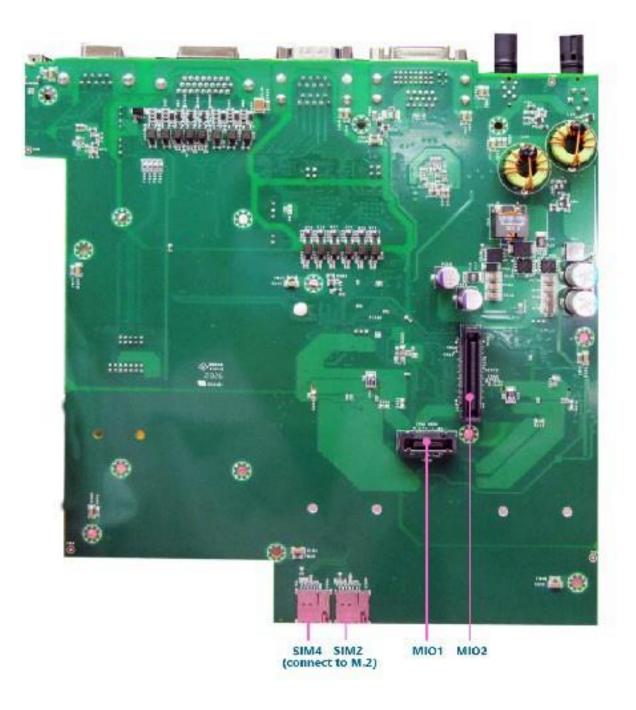


# IO Board Layout (B/C SKU)

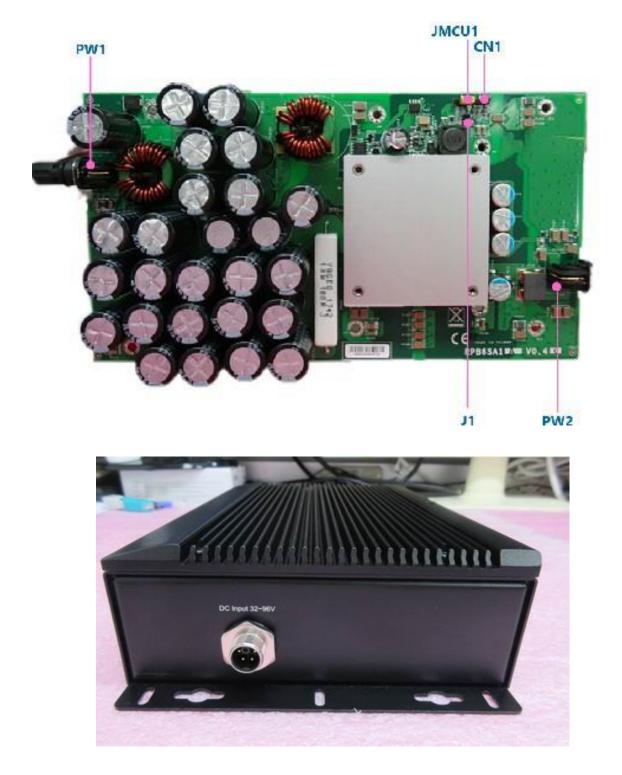
**Front View** 



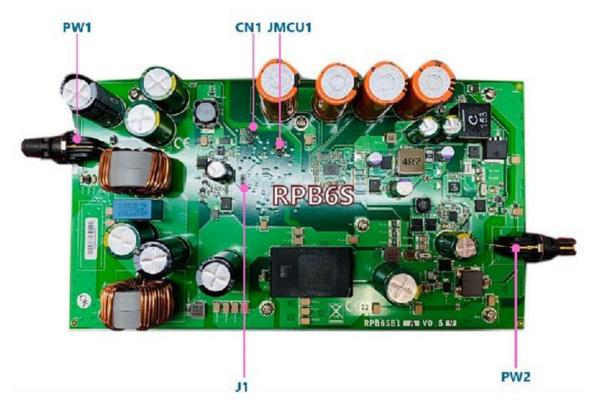
### **Rear View**



# Power Board Layout (A SKU)



# Power Board Layout (B/C SKU)



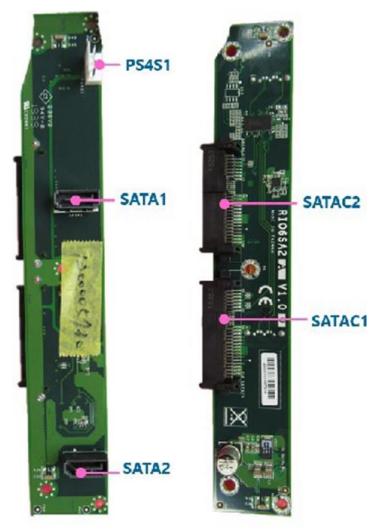
B SKU



C SKU



# I/O Board Layout (A SKU)



# Internal Jumper & Connectors (Motherboard)

1 21

1

20 40

#### MI01

Pin	Signals	Pin	Signals
1	GND	21	GND
2	P3V3	22	DC_IN
3	P3V3	23	DC_IN
4	P3V3	24	DC_IN
5	PSV3	25	DC_IN
6	P3V3	26	DC_IN
7	P3V3	27	DC_IN
8	TP81	28	DC_IN
9	PCH_PWROK	29	DC_IN
10	MCU_PG	30	TP79
11	GND	31	SIO_DGOUT_0
12	SMB_S0_CLK	32	TP80
13	SMB_S0_DAT	33	GND
14	P12V_S8_PG	34	P12V_VIN
15	IGNITION	35	P12V_VIN
16	IGN3V3_SB	36	P12V_SB
17	GND	37	P12V_SB
18	GND	38	P12V_SB
19	P12V_SB	39	P12V_SB
20	P12V_SB	40	P12V_SB

#### MI02

PM_SLP_S3#         51         VCC_CORE           2         HDA_RST#_R         52         HDA_SDI           3         HDA_BLV_R         53         HDA_SDI           4         HDA_SDO_R         54         SPEED           5         HDA_SVNC_R         55         FORWARD           6         GND         56         PLTRST           7         SIO_CLKIN         57         DDIL_DAT           8         SOUT6         58         DDIL_CLK           9         SIN6         59         DDIL_CLK           9         SIN6         59         DDIL_LK           9         SUN6         62         DDIL_LHPD           11         LPC_LAD0         62         DDIL_DAT           13         LPC_LAD1         63         GND           14         LPC_LAD2         65         USB20_NF           16         SIO_CLK_24M         66         USB20_NF           18         SIN3         68         GND           19         PM_SLP_S4#         69         USB20_NF           20         KBRST#         70         USB3_HTX_DRX_N4           25         CPU_PECI         75         USB3_HTX_DRX	Pin	Signals	Pin	Signals
3         HDA_BLK_R         53         HDA_SD0           4         HDA_SD0_R         54         SPEED           5         HDA_SYNC_R         55         FORWARD           6         GND         56         PLTRST           7         SIO_CLKIN         57         DDI1_DAT           8         SOUT6         58         DDI1_CLK           9         SIN6         59         DDI2_LLK           10         LPC_LFRAME#         60         DDI2_HPD           11         LPC_LSERIRQ         61         DDI1_DAT           13         LPC_LAD1         63         GND           14         LPC_LAD2         65         USB20_N7           15         LPC_LAD2         65         USB20_N5           20         KBRST#         70         USB20_N5           20         KBRST#         70         USB20_N5           21         PIV2_VDDQ         71         USB3_HTX_DRX_N4           23         TP77         73         USB3_HTX_DRX_N4           24         RSMEST#         74         USB3_HTX_DRX_N4           25         CPU_PECI         75         USB3_HTX_DRX_N4           26         WDT </td <td>1</td> <td>PM_SUP_S3#</td> <td>51</td> <td></td>	1	PM_SUP_S3#	51	
A         HDA_SDO_R         54         SPEED           5         HDA_STNC_R         55         FORWARD           6         GND         56         PLTRST           7         SIO_CLKIN         57         DDI1_CLK           9         SIN6         59         DDI2_CLK           9         SIN6         59         DDI2_CLK           10         LPC_LFRAME#         60         DDI2_HPD           11         LPC_SERIRQ         61         DDI1_HPD           12         LPC_LAD0         62         DDI2_DAT           13         LPC_LAD1         63         GND           14         LPC_LAD2         65         USB20_N7           15         LPC_LAD2         65         USB20_N6           17         SOUT3         67         USB20_N5           20         KBRST#         70         USB20_N5           20         KBRST#         70         USB20_N5           21         PIV2_VDDQ         71         USB_MTX_DRX_P4           24         RSMBST#         74         USB3_HTX_DRX_P4           25         CPU_PECI         75         USB3_HTX_DRX_P4           26         WDT	2	HDA_RST#_R	52	HDA_SDI1
5         HDA_SYNC_R         55         FORWARD           6         GND         56         PLTRST           7         SIQ_CLKIN         57         DDIL_DAT           8         SOUT6         58         DDIL_LK           9         SIN6         59         DDIL_CLK           10         LPC_LFRAME#         60         DDIL_LK           11         LPC_SERIRQ         61         DDIL_HPD           12         LPC_LAD0         62         DDIL_DAT           13         LPC_LAD1         63         GND           14         LPC_LAD2         65         USB20_N7           15         LPC_LAD2         65         USB20_N5           16         SIO_CLK_24M         66         USB20_N5           20         KBRST#         70         USB20_P5           21         P1VZ_VDDQ         71         USB_CC2#           23         TP77         73         USB3_HTX_DRX_N4           24         RSMRST#         74         USB3_HTX_DRX_N4           25         CPU_PECI         75         USB3_HTX_DRX_N4           26         WDT         76         USB3_HTX_DRX_N4           27         PME#	3	HDA_BLK_R	53	HDA_SDI0
6         GND         56         PLTRST           7         SIQ_CLKIN         57         DDII_DAT           8         SOUT6         58         DDII_CLK           9         SIN6         59         DDI2_CLK           10         LPC_LFRAME#         60         DDI2_HPD           11         LPC_SERIRQ         61         DDI1_HPD           12         LPC_LAD0         62         DDI2_DAT           13         LPC_LAD1         63         GND           14         LPC_LAD2         65         USB20_N7           15         LPC_LAD2         65         USB20_N6           17         SOUT3         67         USB20_N6           18         SIN3         68         GND           19         PM_SUP_S4#         69         USB20_N5           20         KBRST#         70         USB3_CLX_P4           23         TP77         73         USB3_HTX_DRX_P4           24         RSMRST#         74         USB3_HTX_DRX_P4           25         CPU_PECI         75         USB3_HTX_DRX_P3           26         WDT         76         USB3_HTX_DRX_P4           27         PME#	4	HDA_SDO_R	54	SPEED
7         SIO_CLKIN         57         DDI1_DAT           8         SOUT6         58         DDI1_CLK           9         SIN6         59         DDI2_CLK           10         LPC_LFRAME#         60         DDI2_LK           11         LPC_SERIRQ         61         DDI1_HPD           12         LPC_LAD0         62         DDI2_DAT           13         LPC_LAD1         63         GND           14         LPC_LAD2         64         USB20_N7           15         LPC_LAD2         65         USB20_N6           17         SOUT3         67         USB20_N5           18         SIN3         68         GND           19         PM_SLP_S4#         69         USB20_N5           20         KBRST#         70         USB20_N5           21         PIV2_VDDQ         71         USB3_HTX_DRX_P4           24         RSMRST#         74         USB3_HTX_DRX_N4           25         CPU_PECI         75         USB3_HTX_DRX_N4           26         WDT         76         USB3_HTX_DRX_N3           30         EXT_PWR         80         USB3_HTX_DRX_N3           32 <t< td=""><td>5</td><td>HDA_SYNC_R</td><td>55</td><td>FORWARD</td></t<>	5	HDA_SYNC_R	55	FORWARD
8         SOUTE         58         DDIL_CLK           9         SIN6         59         DDIL_CLK           9         SIN6         59         DDIL_CLK           10         LPC_LFRAME#         60         DDIL_HPD           11         LPC_LAD0         62         DDIL_DAT           13         LPC_LAD1         63         GND           14         LPC_LAD2         65         USB20_N7           15         LPC_LAD2         65         USB20_N6           17         SOUT3         67         USB20_N6           18         SIN3         68         GND           19         PM_SLP_S4#         69         USB20_N5           20         KBRST#         70         USB20_N5           21         PIV2_VDDQ         71         USB_OC2#           22         TP78         72         GND           23         TP77         73         USB3_HTX_DRX_N4           26         WDT         76         USB3_HTX_DRX_N4           27         PME#         77         GND           28         MCU_CLK         78         USB3_HTX_DRX_N3           30         EXT_PWR         80	6	GND	56	PLTRST
9         SIN6         59         DDD2_CLK           10         LPC_LFRAME#         60         DD12_HPD           11         LPC_SERIRQ         61         DD11_HPD           12         LPC_LAD0         62         DD12_DAT           13         LPC_LAD1         63         GND           14         LPC_LAD2         65         US820_N7           15         LPC_LAD2         65         US820_N6           17         SOUT3         67         US820_N6           18         SIN3         68         GND           19         PM_SLP_S4#         69         US820_N5           20         KBRST#         70         US820_P5           21         P1V2_VDDQ         71         US8_DC2#           22         TP78         72         GND           23         TP77         73         US83_HTX_DRX_N4           24         RSMRST#         74         US83_HTX_DRX_N4           25         CPU_PECI         75         US83_HTX_DRX_N4           26         WDT         76         US83_HTX_DRX_N4           27         PME#         77         GND           38         MCU_CLK	7	SIO_CLKIN	57	DDI1_DAT
10         LPC_LFRAME#         60         DDI2_HPD           11         LPC_SERIRQ         61         DDI1_HPD           12         LPC_LAD0         62         DDI2_DAT           13         LPC_LAD1         63         GND           14         LPC_LAD2         65         US820_N7           15         LPC_LAD2         65         US820_N6           17         SOUT3         67         US820_N6           18         SIN3         68         GND           18         SIN3         68         GND           19         PM_SLP_S4#         69         US820_N5           20         KBRST#         70         US82_NS           21         P1V2_VDDQ         71         US8_DC3#           22         TP78         72         GND           23         TP77         73         US83_HTX_DRX_N4           24         RSMRST#         74         US83_HTX_DRX_N4           25         CPU_PECI         75         US83_HTX_DRX_N4           26         WDT         76         US83_HTX_DRX_N4           27         PME#         77         GND           28         MCU_CLK         8	8	SOUT6	58	DDI1_CLK
11         LPC_SERIRQ         61         DDII_HPD           12         LPC_LAD0         62         DDI2_DAT           13         LPC_LAD1         63         GND           14         LPC_LAD2         65         US820_P7           15         LPC_LAD2         65         US820_P7           16         SIO_CLK_24M         66         US820_P6           17         SOUT3         67         US820_P6           18         SIN3         68         GND           19         PMSLP_S4#         69         US820_N5           20         KBRST#         70         US820_P5           21         P1V2_VDDQ         71         US8_DC2#           23         TP77         73         US83_HTX_DRX_P4           24         RSMRST#         74         US83_HTX_DRX_P4           25         CPU_PECI         75         US83_HTX_DRX_P4           26         WDT         76         US83_HTX_DRX_N3           27         PME#         77         GND           28         MCU_CLK         78         US83_HTX_DRX_N3           30         EXT_PWR         80         US83_HTX_DRX_N3           38	9	SIN6	59	DDI2_CLK
12         LPC_LAD0         62         DDI2_DAT           13         LPC_LAD1         63         GND           14         LPC_LAD3         64         USS20_N7           15         LPC_LAD2         65         USS20_N7           16         SIO_CLK_24M         66         USS20_N6           17         SOUT3         67         USS20_N6           18         SIN3         68         GND           19         PM_SUP_S4#         69         USS20_N5           20         KBRST#         70         USS8_O_N5           21         P1V2_VDDQ         71         US8_OC2#           22         TP78         72         GND           23         TP77         73         US83_HTX_DRX_N4           25         CPU_PECI         75         US83_HTX_DRX_N4           26         WDT         76         US83_HTX_DRX_N3           30         EXT_PWR         80         US83_HTX_DRX_N3           31         MCU_DAT         81         US83_HTX_DRX_N3           32         GND         82         GND           33         DDI2_TXP3         85         CLK_PCIE_P4_MIO           34         DDI2	10	LPC_LFRAME#	60	DDI2_HPD
13         LPC_LAD1         63         GND           14         LPC_LAD3         64         US820_N7           15         LPC_LAD2         65         US820_P7           16         SIO_CLK_24M         66         US820_N6           17         SOUT3         67         US820_N6           18         SIN3         68         GND           19         PM_SLP_54#         69         US820_N5           20         KBRST#         70         US820_P5           21         PIV2_VDDQ         71         US8_OC2#           22         TP78         72         GND           23         TP77         73         US83_HTX_DRX_N4           25         CPU_PECI         75         US83_HTX_DRX_N4           26         WDT         76         US83_HTX_DRX_N4           27         PME#         77         GND           28         MCU_CLK         78         US83_HTX_DRX_N3           30         EXT_PWR         80         US83_HTX_DTX_N3           31         MCU_DAT         81         US83_HRX_DTX_N3           32         GND         82         GND           33         DDI2_TXN2	11	LPC_SERIRQ	61	DDI1_HPD
14         LPC_LAD3         64         US820_N7           15         LPC_LAD2         65         US820_P7           16         SIO_CLK_24M         66         US820_N6           17         SOUT3         67         US820_N6           18         SIN3         68         GND           19         PM_SLP_S4#         69         US820_N5           20         KBRST#         70         US820_P5           21         P1V2_VDDQ         71         US8_OC2#           22         TP78         72         GND           23         TP77         73         US83_HTX_DRX_N4           24         RSMRST#         74         US83_HTX_DRX_N4           25         CPU_PECI         75         US83_HTX_DRX_N4           26         WDT         76         US83_HTX_DRX_N3           27         PME#         77         GND         28           MCU_CLK         78         US83_HTX_DRX_N3         30         EXT_PWR         80         US83_HTX_DRX_N3           38         DDI2_TXP2         83         CLK_PCIE_P4_MID         34         DDI2_TXP3         85         GND           37         DDI2_TXP3         85	12	LPC_LAD0	62	DDI2_DAT
15         LPC_LAD2         65         US820_P7           16         SIO_CLK_24M         66         US820_N6           17         SOUT3         67         US820_P6           18         SIN3         68         GND           19         PM_SLP_54#         69         US820_N5           20         KBRST#         70         US820_P5           21         P1V2_VDDQ         71         US8_OC2#           23         TP77         73         US83_HTX_DRX_P4           24         RSMRST#         74         US83_HTX_DRX_P4           24         RSMRST#         74         US83_HTX_DRX_P4           24         RSMRST#         74         US83_HTX_DRX_N4           25         CPU_PECI         75         US83_HTX_DRX_N4           26         WDT         76         US83_HTX_DRX_N3           30         EXT_PWR         80         US83_HTX_DRX_N3           30         EXT_PWR         80         US83_HTX_DTX_N3           31         MCU_LAT         81         US83_HTX_DTX_N3           32         GIND         85         GIND           33         DDI2_TXN3         86         PCIE_HTX_DRX_N5 <t< td=""><td>13</td><td>LPC_LAD1</td><td>63</td><td>GND</td></t<>	13	LPC_LAD1	63	GND
16         SIO_CLK_24M         66         USB20_N6           17         SOUT3         67         USB20_P6           18         SIN3         68         GND           19         PM_SLP_54#         69         USB20_N5           20         KBRST#         70         USB20_P5           21         PIV2_VDDQ         71         USB2_OC2#           22         TP78         72         GND           23         TP77         73         USB3_HTX_DRX_P4           24         RSMRST#         74         USB3_HTX_DRX_P4           25         CPU_PECI         75         USB3_HTX_DRX_P4           26         WDT         76         USB3_HTX_DRX_P3           27         PME#         77         GND           28         MCU_CLK         78         USB3_HTX_DRX_P3           30         EXT_PWR         80         USB3_HTX_DRX_P3           31         MCU_DAT         81         USB3_HTX_DRX_N3           32         GND         82         GND           33         DDI2_TXP3         85         GND           34         DDI2_TXN3         86         PCIE_HTX_DRX_N5           37	14	LPC_LAD3	64	US820_N7
16         SIO_CLK_24M         66         USB20_N6           17         SOUT3         67         USB20_P6           18         SIN3         68         GND           19         PM_SLP_54#         69         USB20_N5           20         KBRST#         70         USB20_P5           21         PIV2_VDDQ         71         USB2_OC2#           22         TP78         72         GND           23         TP77         73         USB3_HTX_DRX_P4           24         RSMRST#         74         USB3_HTX_DRX_P4           25         CPU_PECI         75         USB3_HTX_DRX_P4           26         WDT         76         USB3_HTX_DRX_P3           27         PME#         77         GND           28         MCU_CLK         78         USB3_HTX_DRX_P3           30         EXT_PWR         80         USB3_HTX_DRX_P3           31         MCU_DAT         81         USB3_HTX_DRX_N3           32         GND         82         GND           33         DDI2_TXP3         85         GND           34         DDI2_TXN3         86         PCIE_HTX_DRX_N5           37	15	LPC_LAD2	65	US820_P7
18         SIN3         68         GND           19         PM_SLP_S4#         69         US820_NS           20         KBRST#         70         US820_PS           21         PIV2_VDDQ         71         US8_OC2#           22         TP78         72         GND           23         TP77         73         US83_HTX_DRX_P4           24         RSMRST#         74         US83_HTX_DRX_N4           25         CPU_PECI         75         US83_HTX_DTX_N4           26         WDT         76         US83_HTX_DRX_N4           27         PM6#         77         GND           28         MCU_CLK         78         US83_HTX_DRX_N3           30         EXT_PWR         80         US83_HTX_DTX_N3           31         MCU_DAT         81         US83_HRX_DTX_N3           32         GND         82         GND           33         DDI2_TXP3         85         CIL           34         DDI2_TXN3         86         PCIE_HTX_DRX_N5           37         DDI2_TXN0         87         PCIE_HTX_DRX_N5           38         DIQ_TXN1         90         GND           39 <t< td=""><td>16</td><td></td><td>66</td><td>US820_N6</td></t<>	16		66	US820_N6
19         PM_SLP_S4#         69         US820_NS           20         KBRST#         70         US820_PS           21         P1V2_VDDQ         71         US8_0C2#           22         TP78         72         GND           23         TP77         73         US83_HTX_DRX_P4           24         RSMRST#         74         US83_HTX_DRX_P4           24         RSMRST#         74         US83_HTX_DRX_N4           25         CPU_PECI         75         US83_HTX_DRX_N4           26         WDT         76         US83_HTX_DRX_N4           27         PME#         77         GND           28         MCU_CLK         78         US83_HTX_DRX_N3           30         EXT_PWR         80         US83_HTX_DRX_N3           30         EXT_PWR         80         US83_HRX_DTX_N3           31         MCU_CLAT         81         US83_HRX_DTX_N3           32         GND         82         GND           33         DDI2_TXP3         85         GND           34         DDI2_TXP3         85         GND           35         DDI2_TXP3         85         PCIE_HTX_DRX_P5           38<	17	SOUT3	67	USB20_P6
20         KBRST#         70         US820_P5           21         P1V2_VDDQ         71         US8_0C2#           22         TP78         72         GND           23         TP77         73         US8_JHTX_DRX_P4           24         RSMRST#         74         US8_JHTX_DRX_P4           24         RSMRST#         74         US8_JHTX_DRX_P4           25         CPU_PECI         75         US83_HTX_DRX_P4           26         WDT         76         US83_HTX_DRX_P4           27         PME#         77         GND           28         MCU_CLK         78         US83_HTX_DRX_P3           29         DGIN_0_MCU         79         US83_HTX_DRX_N3           30         EXT_FWR         80         US83_HTX_DRX_N3           31         MCU_DAT         81         US83_HTX_DRX_N3           32         GIND         82         GND           33         DDI2_TXN2         84         CLK_PCIE_P4_MIO           34         DDI2_TXN3         85         GND           35         DDI2_TXN3         85         GND           36         DDI2_TXN3         86         PCIE_HTX_DRX_N5	18	SINB	68	GND
21         P1V2_VDDQ         71         US8_OC2#           22         TP78         72         GND           23         TP77         73         US83_HTX_DRX_P4           24         RSMRST#         74         US83_HTX_DRX_P4           25         CPU_PECI         75         US83_HTX_DRX_P4           26         WDT         76         US83_HTX_DRX_P4           27         PME#         77         GND           28         MCU_CLK         78         US83_HTX_DRX_P3           29         DGIN_0_MCU         79         US83_HTX_DRX_P3           30         EXT_PWR         80         US83_HTX_DRX_P3           31         MCU_DAT         81         US83_HTX_DRX_P3           32         GND         82         GND           33         DDI2_TXP3         85         GND           34         DDI2_TXP3         85         GND           35         DDI2_TXP3         86         PCIE_HTX_DRX_N5           37         DDI2_TXP1         89         PCIE_HTX_DRX_N6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N5           39         DDI2_TXP1         90         GND	19	PM_SLP_S4#	69	US820_N5
22         TP78         72         GND           23         TP77         73         US83,HTX_DRX_P4           24         RSMRST#         74         US83,HTX_DRX_P4           25         CPU_PECI         75         US83,HTX_DRX_P4           26         WDT         76         US83,HTX_DRX_P4           27         PME#         77         GND           28         MCU_CLK         78         US83,HTX_DRX_P3           29         DGIN_0,MCU         79         US83,HTX_DRX_N3           30         EXT_PWR         80         US83,HTX_DRX_N3           31         MCU_DAT         81         US83,HTX_DRX_N3           32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCIE_P4_MIO           34         DDI2_TXP3         85         GND           35         DDI2_TXN2         84         CLK_PCIE_P4_MIO           36         DDI2_TXN0         87         PCIE_HTX_DRX_N5           37         DDI2_TXN0         86         PCIE_HTX_DRX_N6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           39         DDI2_TXN1         90         GND <td>20</td> <td>KBRST#</td> <td>70</td> <td>US820_P5</td>	20	KBRST#	70	US820_P5
22         TP78         72         GND           23         TP77         73         US83,HTX_DRX_P4           24         RSMRST#         74         US83,HTX_DRX_P4           25         CPU_PECI         75         US83,HTX_DRX_P4           26         WDT         76         US83,HTX_DRX_P4           27         PME#         77         GND           28         MCU_CLK         78         US83,HTX_DRX_P3           29         DGIN_0,MCU         79         US83,HTX_DRX_N3           30         EXT_PWR         80         US83,HTX_DRX_N3           31         MCU_DAT         81         US83,HTX_DRX_N3           32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCIE_P4_MIO           34         DDI2_TXP3         85         GND           35         DDI2_TXN2         84         CLK_PCIE_P4_MIO           36         DDI2_TXN0         87         PCIE_HTX_DRX_N5           37         DDI2_TXN0         86         PCIE_HTX_DRX_N6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           39         DDI2_TXN1         90         GND <td>21</td> <td>P1V2_VDDQ</td> <td>71</td> <td>USB_OC2#</td>	21	P1V2_VDDQ	71	USB_OC2#
24         RSMRST#         74         USB3_HTX_DRV_N4           25         CPU_PECI         75         USB3_HRX_DTX_N4           26         WDT         76         USB3_HRX_DTX_N4           26         WDT         76         USB3_HRX_DTX_N4           27         PME#         77         GND           28         MCU_CLK         78         USB3_HTX_DRX_P3           29         DGIN_0_MCU         79         USB3_HTX_DRX_N3           30         EXT_FWR         80         USB3_HRX_DTX_N3           31         MCU_DAT         81         USB3_HRX_DTX_N3           32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCIE_P4_MIO           34         DDI2_TXN3         86         PCIE_HTX_DRX_N5           37         DDI2_TXN3         86         PCIE_HTX_DRX_N6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           39         DDI2_TXN1         90         GND           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_N5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5 <td>22</td> <td>TP78</td> <td>72</td> <td></td>	22	TP78	72	
25         CPU_PECI         75         USB3_HRX_DTX_N4           26         WDT         76         USB3_HRX_DTX_P4           27         PME#         77         GND           28         MCU_CLK         78         USB3_HTX_DRX_P3           29         DGIN_0_MCU         79         USB3_HTX_DRX_P3           30         EXT_PWR         80         USB3_HTX_DRX_P3           31         MCU_DAT         81         USB3_HTX_DTX_P3           32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCIE_N4_MIO           34         DDI2_TXP3         85         GND           35         DDI2_TXP3         85         GND           36         DDI2_TXP3         86         PCIE_HTX_DRX_P5           37         DDI2_TXP1         89         PCIE_HTX_DRX_N6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXP1         90         GND           41         GND         91         PCIE_HRX_DTX_N5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	23	TP77	73	US83_HTX_DRX_P4
25         CPU_PECI         75         USB3_HRX_DTX_N4           26         WDT         76         USB3_HRX_DTX_P4           27         PMB#         77         GND           28         MCU_CLK         78         USB3_HTX_DRX_P3           29         DGIN_0_MCU         79         USB3_HTX_DRX_P3           30         EXT_PWR         80         USB3_HTX_DRX_P3           31         MCU_DAT         81         USB3_HTX_DRX_P3           32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCIE_P4_MIO           34         DDI2_TXP3         85         GND           35         DDI2_TXP3         85         GND           36         DDI2_TXN3         86         PCIE_HTX_DRX_P5           37         DDI2_TXN0         87         PCIE_HTX_DRX_P6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_P5           42         DDI1_TXN0         92         PCIE_HRX_DTX_P5	24	RSMRST#	74	USB3_HTX_DRX_N4
27         PME#         77         GND           28         MCU_CLK         78         USB3_HTX_DRX_P3           29         DGIN_0_MCU         79         USB3_HTX_DRX_N3           30         EXT_PWR         80         USB3_HTX_DTX_N3           31         MCU_DAT         81         USB3_HTX_DTX_N3           32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCIE_P4_MIO           34         DDI2_TXP3         85         GND           36         DDI2_TXP3         86         PCIE_HTX_DRX_N5           37         DDI2_TXP0         88         PCIE_HTX_DRX_N5           38         DDI2_TXP1         89         PCIE_HTX_DRX_N6           39         DDI2_TXP1         88         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_N5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	25	CPU_PECI	75	
28         MCU_CLK         78         US83_HTX_DRX_P3           29         DGIN_0_MCU         79         US83_HTX_DRX_N3           30         EXT_PWR         80         US83_HTX_DTX_N3           31         MCU_DAT         81         US83_HTX_DTX_N3           32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCIE_P4_MIO           34         DDI2_TXP3         84         CLK_PCIE_N4_MIO           35         DDI2_TXP3         85         GND           36         DDI2_TXN3         86         PCIE_HTX_DRX_P5           37         DDI2_TXN0         87         PCIE_HTX_DRX_P6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXP1         90         GND           41         GND         91         PCIE_HTX_DTX_N5           42         DDI1_TXN0         92         PCIE_HTX_DTX_N5	26	WDT	76	USB3_HRX_DTX_P4
29         DGIN_0_MCU         79         USB3_HTX_DRX_N3           30         EXT_PWR         80         USB3_HRX_DTX_N3           31         MCU_DAT         81         USB3_HRX_DTX_P3           32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCIE_P4_MIO           34         DDI2_TXP3         84         CLK_PCIE_N4_MIO           35         DDI2_TXP3         85         GND           36         DDI2_TXN3         86         PCIE_HTX_DRX_N5           37         DDI2_TXN0         87         PCIE_HTX_DRX_P5           38         DDI2_TXP0         88         PCIE_HTX_DRX_N6           39         DDI2_TXN1         90         GND           40         DI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_P5           42         DDI1_TXN0         92         PCIE_HRX_DTX_P5	27	PME#	77	GND
30         EXT_PWR         80         USB3_HRX_DTX_N3           31         MCU_DAT         81         USB3_HRX_DTX_P3           32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCIE_P4_MIO           34         DDI2_TXP3         84         CLK_PCIE_N4_MIO           35         DDI2_TXP3         85         GND           36         DDI2_TXN3         86         PCIE_HTX_DRX_N5           37         DDI2_TXN0         87         PCIE_HTX_DRX_N5           38         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_N5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5			78	
30         EXT_PWR         80         USB3_HRX_DTX_N3           31         MCU_DAT         81         USB3_HRX_DTX_P3           32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCIE_P4_MIO           34         DDI2_TXP3         84         CLK_PCIE_N4_MIO           35         DDI2_TXP3         85         GND           36         DDI2_TXN3         86         PCIE_HTX_DRX_N5           37         DDI2_TXN0         87         PCIE_HTX_DRX_N5           38         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_N5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	29	DGIN_0_MCU	79	USB3_HTX_DRX_N3
31         MCU_DAT         81         USB3_HRX_DTX_P3           32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCIE_P4_MIO           34         DDI2_TXP2         84         CLK_PCIE_P4_MIO           35         DDI2_TXP3         84         CLK_PCIE_N4_MIO           36         DDI2_TXP3         85         GND           37         DDI2_TXP0         87         PCIE_HTX_DRX_N5           38         DDI2_TXP1         89         PCIE_HTX_DRX_N6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_N5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	30	EXT_PWR	80	
32         GND         82         GND           33         DDI2_TXP2         83         CLK_PCE_P4_MIO           34         DDI2_TXP2         84         CLK_PCE_P4_MIO           35         DDI2_TXP3         85         GND           36         DDI2_TXP3         85         GND           37         DDI2_TXN0         87         PCIE_HTX_DRX_N5           38         DDI2_TXP1         88         PCIE_HTX_DRX_N6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_N5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	31		81	USB3_HRX_DTX_P3
34         DDI2_TXN2         84         CLK_PCIE_N4_MIO           35         DDI2_TXP3         85         GND           36         DDI2_TXN3         86         PCIE_HTX_DRX_N5           37         DDI2_TXN0         87         PCIE_HTX_DRX_P5           38         DDI2_TXP0         88         PCIE_HTX_DRX_P6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_P5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	32		82	
35         DDI2_TXP3         85         GND           36         DDI2_TXN3         86         PCIE_HTX_DRX_N5           37         DDI2_TXN0         87         PCIE_HTX_DRX_P5           38         DDI2_TXP0         88         PCIE_HTX_DRX_P6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_P5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	33	DDI2_TXP2	83	CLK_PCIE_P4_MIO
36         DDI2_TXN3         86         PCIE_HTX_DRX_N5           37         DDI2_TXN0         87         PCIE_HTX_DRX_P5           38         DDI2_TXP0         88         PCIE_HTX_DRX_P6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_P5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	34	DDI2_TXN2	84	CLK POE N4 MIO
37         DDI2_TXN0         87         PCIE_HTX_DRX_P5           38         DDI2_TXP0         88         PCIE_HTX_DRX_P6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_P5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	35	DDI2_TXP3	85	GND
37         DDI2_TXN0         87         PCIE_HTX_DRX_P5           38         DDI2_TXP0         88         PCIE_HTX_DRX_P6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_P5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	36	DDI2 TXN3	86	PCIE HTX DRX NS
38         DDI2_TXP0         88         PCIE_HTX_DRX_P6           39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_P5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5				
39         DDI2_TXP1         89         PCIE_HTX_DRX_N6           40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_P5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	38	DDI2_TXP0	88	
40         DDI2_TXN1         90         GND           41         GND         91         PCIE_HRX_DTX_P5           42         DDI1_TXN0         92         PCIE_HRX_DTX_N5	39		89	
41 GND 91 PCIE_HRX_DTX_P5 42 DDI1_TXN0 92 PCIE_HRX_DTX_N5	_		90	
42 DDI1_TXN0 92 PCIE_HRX_DTX_N5	41		91	PCIE_HRX_DTX_PS
	42	DDI1_TXN0	92	
	43	DDI1_TXP0	93	PCIE_HRX_DTX_P6
44 DDI1_TXN1 94 PCIE_HRX_DTX_N6	44		94	
45 DDI1_TXP1 95 GND			95	
46 DDI1_TXP2 96 DDI2_AUX_N	46			
47 DDI1_TXN2 97 DDI2_AUX_P		DDI1_TXN2	97	DDI2_AUX_P
48 DDI1_TXP3 98 DDI1_AUX_P	48		98	
49 DDI1_TXN3 99 DDI1_AUX_N	49		99	
50 GND 100 GND	50		100	

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n	Signals	Pin	Signals	1	10.0	10	10
1	P5V	6	GND	2	20	200	9
2	PSV	7	GND		-		100
3	P3V3	8	GND	+			8 💭
	PSV	9	GND	5			7 (11)
;	GND	10	GND	1		6	
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in							
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2	SATA_HTX_ SATA_HTX_I			- 22			
	GND		<b>-</b>	- 22			
;	SATA_HRX		0	- 22			
5	SATA HRX						
7	GND		-	7 🌑			
TA	2 (IN)						
in	Signa	als		1.05			
	GND		_				
2	SATA_HTX			- 65			
	SATA_HTX_I		1	- 65			
5	GND SATA_HRX_		-				
5	SATA_HRX	_		- 21			
_			·	7 🔍			
7	GND						
A1	TA1 Signals		in	Signals		1	22
'n	Signals	P		Signals		1	
n		P	in 2	Signals P3V3 GND		1	
n	Signals x	P	2 4	P3V3		1	
n	Signals x x	P	2 4	P3V3 GND		1	
	Signals x x x x GND	P	2 4 6 P1 8 10	P3V3 GND IV5_MPCIE X		1	222222
n 	Signals x x x x GND x	P	2 4 6 Pt 8 10 12	P3V3 GND IVS_MPCIE X X		1	2222222
n 3	Signals x x x x GND x x x	P	2 4 6 P1 8 8 10 12 14 14 14 14 14 14 14 14 14 14 14 14 14	P3V3 GND V5_MPCIE X X X X		1	22222222
n 3	Signals x x x GND x x GND x GND	P	2 4 6 P1 8 10 12 14 14 14 14 14 14 14 14 14 14 14 14 14	P3V3 GND IV5_MPCIE X X X X X		1	1222222222
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n 1 3 5 7 9 1 3 5 7 9 1	Signals x x x GND x GND x x GND SATA_HRX_C GND SATA_HRX_C GND GND SATA_HRX_C GND SATA_HTX_C SATA_HTX_C DTXN2 SATA_HTX_C	P 3 4 1 1 1 1 1 1 2 2 2 2 2 2 2 2 3 3 3 3 3 3	2 4 4 9 6 P1 8 9 12 14 14 16 18 9 14 16 16 18 18 9 14 16 18 9 19 5 10 5 10 10 5 10 10 10 5 10 10 10 10 10 10 10	P3V3 GND VS_MPCIE X X X GND X P3V3 GND VS_MPCIE WB_S0_CLK		1	
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n 3 5 7 9 1 3 5 7 9 1 3 5 7 9 1 3 5 5 7 9 1 3 5 5 7 9 1	Signals x x x GND x GND x x GND x x GND X SATA_HTX_C DTXN2 GND GND GND GND GND GND GND GND	P 3 4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	2 4 4 9 6 94 8 9 10	P3V3 GND VS_MPCIE X X X GND X P3V3 GND VS_MPCIE VB_S0_CLK KB_S0_DAT GND		1	
n 3 5 7 9 1 3 5 7 9 1 3 5 7 9 1 3 5 7 9 1 3 5 7 9 1 3 5 7 9 1 3 5 7 9 1 3 5 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 3 5 7 7 9 1 1 7 7 9 1 7 7 7 9 1 7 7 7 9 1 7 7 7 9 1 7 7 7 9 1 7 7 7 7 9 1 7 7 7 9 1 7 7 7 9 1 7 7 7 7 9 1 7 7 7 9 1 7 7 7 7 9 1 7 7 7 7 7 7 7 7 7 9 1 7 7 7 7 7 7 7 7 7 7 7 7 7	Signals X X X GND X GND X GND X SATA_HRX_C DTXP2 GND GND SATA_HRX_C DTXP2 GND SATA_HRX_C DTXP2 GND SATA_HRX_C DTXP2 GND SATA_HRX_C DTXP2 GND SATA_HRX_C DTXP2 GND SATA_HRX_C DTXP2 GND	P 	2 4 4 9 10 0 12 14 14 16 18 8 10 12 14 16 16 19 14 19 16 19 14 19 16 19 10 51 11 19 12 55 14 19 14 19 15 19 16 19 17 19 18 19 19 19 1	P3V3 GND IV5_MPCIE X X X GND IV5_MPCIE MB_50_CLK AB_50_DAT GND X		1	
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#### LAN14~LAN13

Pin	Signals	Pin	Signals
1	LANX_MX0P	8	LANK_MX2P
2	LANX_MX0N	7	LANX_MX2N
3	LANX_MX1P	6	LANX_MX3P
4	LANX_MX1P	5	LANK_MX3P



# Internal Jumper & Connectors (IO Board)

#### MPCIE1 & MPCIE2

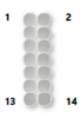
Pin	Signals	Pin	Signals	
1	E_WAKE1	2	P3V3_WLAN1	1 68
3	x	4	GND	
5	x	6	P1V5_MPCIE1	
7	UIM1_RST2	8	UIM1_PWR	
9	GND	10	UIM1_RST1	
11	CLK_PCIE_N_MPCIE1_SW	12	UIM1_CLK1	
13	CLK_PCIE_P_MPCIE1_SW	14	UIM1_DAT1	
15	GND	16	UIM1_VPP1	
17	UIM1_CLK2	18	GND	
19	UIM1_DAT2	20	x	
21	GND	22	x	
23	PCIE_HRX_R_DTX_PS	24	P3V3_WLAN1	
25	PCIE_HRX_R_DTX_NS	26	GND	
27	GND	28	P1V5_MPCIE1	
29	GND	30	E_SCLK	
31	PCIE_HTX_R_DRX_N5	32	E_SDTA	
33	PCIE_HTX_R_DRX_PS	34	GND	
35	GND	36	US820_PS_R	
37	GND	38	US820_N5_R	
39	P3V3_WLAN1	40	GND	
41	P3V3_WLAN1	42	LED_WWAN1-	
43	GND	44	LED_WLAN1-	
45	x	46	x	
47	x	48	P1V5_MPCIE1	
49	x	50	GND	
51	x	52	P3V3_WLAN1	53 👘
53	GND	54	GND	10 5/5

#### CAN(CN1)

2

54

Pin	Signals	Pin	Signals
1	BAT_12V_24V	2	x
з	DO	4	x
5	GND_CANB	6	GND_CANB
7	TP TP28	8	J1850+/J1708+
9	SIN5	10	J1850-/J1708-
11	SOUTS	12	CAN_H/J1939+
13	P5V	14	CAN_L/J1939-



#### CAN(CANB1)

Pin	Signals	Pin	Signals
1	J1850-/J1708-	2	J1850-/J1708-
3	GND	4	J1850+/J1708+
5	CAN_H/J1939+	6	J1850+/J1708+
7	x	8	AT_12V_24V
9	CAN_L/J1939-	10	x



1 (

4 (

PW2 (DC\_OUT)





# Internal Jumper & Connectors (RIOSA2)

#### SATAC1 (OUT)

Pin	Signals
S1	GND
S2	RD_SATA_HTX_DRX_P0
\$3	RD_SATA_HTX_DRX_N0
S4	GND
S5	RD_SATA_HRX_DTX_N0
S6	RD_SATA_HRX_DTX_P0
<b>S7</b>	GND
P1	TP1
P2	TP1
P3	TP1
P4	GND
PS	GND
P6	GND
P7	P5V
P8	P5V
P9	P5V
P10	GND
P11	TP
P12	GND
P13	P12V
P14	P12V
P15	P12V

S1	- 6	
	- 2	
	- 2	
	. 0	
	- 6	
	- 2	
	. 1	
57		
P1		
	- 6	
	- 2	
	. 6	
	- 2	
	. 1	
	. 6	
	1	
	- 2	
	- 6	
	- 2	
	- 6	
DIC		
P15		

PS4S1	PS4S1		
Pin	Signals		
1	P12V		
2	GND		
3	GND		
4	P5V		

#### SATAC2 (OUT)

	C2 (001)	51
Pin	Signals	31
51	GND	
S2	RD_SATA_HTX_DRX_P1	
\$3	RD_SATA_HTX_DRX_N1	
S4	GND	
S5	RD_SATA_HRX_DTX_N1	57
<b>S6</b>	RD_SATA_HRX_DTX_P1	
S7	GND	P1
P1	TP2	
P2	TP2	
P3	TP2	
P4	GND	
PS	GND	
P6	GND	
P7	PSV	
P8	PSV	
P9	PSV	
P10	GND	
P11	TP	
P12	GND	
P13	P12V	
P14	P12V	P15
P15	P12V	

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# Internal Jumper & Connectors (Power Board)

### <u>RPB6S1</u>

### PW1 (DC\_IN)

Pin	Signals		
1	GND		
2	DC_IN		
3	GND		
4	IGN_IN		
5	CHASSIS GND		



4

### PW2 (DC\_OUT)

Pin	Signals		
1	IGN_OUT		
2	MCU_PG		
3	DC 54V Output		
4	GND		
5	CHASSIS GND		

### <u>RPB6SB1</u>

#### CN1

Pin	Signals
1	EXT_TXD_R
2	GND_PSEDCIN_1
3	EXT_RXD_R

#### JMCU1

Pin	Signals
1	IGN3V3_SB
2	PIO_1
3	GND_PSEDCIN_1





# **CHAPTER 2 : HARDWARE SETUP**

# **Hard Disk Installation**

To install the hard disk,

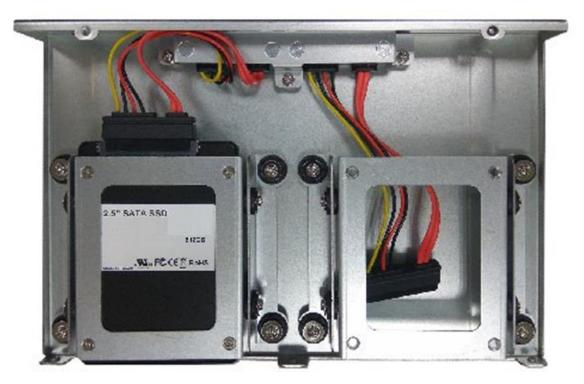
- 1. Loosen the two hand screws that secure the hard disk tray.
- 2. Pull out the tray as shown in the picture below.



3. Remove the screws shown in the picture in order to open the tray.



4. Install the disk onto the tray, and connect the SATA cable. Then, repeat the same steps to install the other disk.



5. Lock the disk tray into the system chassis.

# CHAPTER 3 : SOFTWARE SETUP BIOS Setup

BIOS is a firmware embedded on an exclusive chip on the system's motherboard. Lanner's BIOS firmware offering including market-proven technologies such as Secure Boot and Intel Boot Guard technology deliver solid commitments for the shield protection against malware, uncertified sequences and other named cyber threats. BIOS update for Lanner PCs are available for download <u>here</u>.

### **Entering Setup**

To enter the BIOS setup utility, simply follow the steps below:

1. Boot up the system.

2. Pressing the <Tab> or <Del> key immediately allows you to enter the Setup utility, and then you will be directed to the BIOS main screen. The instructions for BIOS navigations are as below:

Control Keys	Description
→←	select a setup screen, for instance, [Main], [Advanced], [IntelRCSetup], [Security],
	[Boot], and [Save & Exit]
$\uparrow \downarrow$	select an item/option on a setup screen
<enter></enter>	select an item/option or enter a sub-menu
+/-	to adjust values for the selected setup item/option
F1	to display General Help screen
F2	to retrieve previous values, such as the parameters configured the last time you
F2	had entered BIOS.
F3	to load optimized default values
F4	to save configurations and exit BIOS
<esc></esc>	to exit the current screen

# Main Page

Setup main page contains BIOS information and project version information.

BIOS Information		Set the Date. Use Tab
BIOS Vendor	American Megatrends	to switch between Date
Core Version	5.12 0.47 ×64	elements.
Compliancy	UEFI 2.6; PI 1.4	
BIOS Version	FR6SB00000006T205	
Build Date and Time	07/02/2018 12:00:17	
Access Level	Administrator	
System Date	[Sun 01/01/2017]	
System Time	[00:00:40]	-
		→+: Select Screen
		<b>1↓</b> : Select Item
		Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit

AB

Feature	Description	
	BIOS Vendor: American Megatrends	
	Core Version: AMI Kernel version, CRB code base, X64	
	Compliancy: UEFI version, PI version	
BIOS Information	Project Version: BIOS release version	
	Build Date and Time: MM/DD/YYYY	
	Access Level: Administrator / User	
	To set the Date, use <b><tab></tab></b> to switch between Date elements. Default Range	
System Data	of Year: 2005-2099	
System Date	Default Range of Month: 1-12	
	Days: dependent on Month.	
System Time	To set the Date, use <b><tab></tab></b> to switch between Date elements.	

# **Advanced Page**

Select the **Advanced** menu item from the BIOS setup screen to enter the "Advanced" setup screen. Users can select any of the items in the left frame of the screen.

Aptio Setup Utility – Copyright (C) 2018 Am Main Advanced Chipset Security Boot Save	
<ul> <li>CPU Configuration</li> <li>Power &amp; Performance</li> <li>PCH-FW Configuration</li> <li>Trusted Computing</li> <li>Super IO Configuration</li> <li>Hardware Monitor</li> <li>LTE WiFi Selector Setting</li> <li>Status LED Configuration</li> <li>Serial Port Console Redirection</li> </ul>	CPU Configuration Parameters
<ul> <li>Intel TXT Information</li> <li>PCI Subsystem Settings</li> <li>Network Stack Configuration</li> <li>CSM Configuration</li> <li>NVMe Configuration</li> <li>USB Configuration</li> </ul>	<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>
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### **CPU Configuration**

Aptio Setup Utilit Advanced	y – Copyright (C) 2018 Amer	rican Megatrends, Inc.
CPU Configuration		▲ Enable/Disable Software Guard Extensions (SGX)
Type ID Speed L1 Data Cache L1 Instruction Cache L2 Cache L3 Cache	Intel(R) Core(TM) i7-7600U CPU @ 2.80GHz 0x806E9 2900 MHz 32 KB x 2 32 KB x 2 256 KB x 2 4 MB	
L3 Cache L4 Cache Microcode Revision VMX SMX/TXT	N/A 8E Supported Supported	<pre>++: Select Screen f↓: Select Item Enter: Select +/-: Change Opt. F1: General Help</pre>
SW Guard Extensions (SGX)	[Disable]	F2: Previous Values F3: Optimized Defaults ▼ F4: Save & Exit ESC: Exit
Version 2.18.1263	. Copyright (C) 2018 Americ	can Megatrends, Inc. AB
Aptio Setup Utility Advanced	y – Copyright (C) 2018 Ame	rican Megatrends, Inc.
Advanced CPU Flex Ratio	y – Copyright (C) 2018 Amer [Disable]	AP threads Handoff to
Advanced CPU Flex Ratio Override CPU Flex Ratio		
Advanced CPU Flex Ratio Override CPU Flex Ratio Settings Hardware Prefetcher	(Disable) 29	AP threads Handoff to OS Manner from end of
Advanced CPU Flex Ratio Override CPU Flex Ratio Settings Hardware Prefetcher Adjacent Cache Line Prefetch Intel (VMX) Virtualization	[Disable] 29 [Enabled]	AP threads Handoff to OS Manner from end of
Advanced CPU Flex Ratio Override CPU Flex Ratio Settings Hardware Prefetcher Adjacent Cache Line Prefetch Intel (VMX)	[Disable] 29 [Enabled] [Enabled]	AP threads Handoff to OS Manner from end of
Advanced CPU Flex Ratio Override CPU Flex Ratio Settings Hardware Prefetcher Adjacent Cache Line Prefetch Intel (VMX) Virtualization Technology Active Processor Cores Hyper-Threading BIST AP threads Idle	[Disable] 29 [Enabled] [Enabled] [Enabled]	<ul> <li>AP threads Handoff to OS Manner from end of POST</li> <li>++: Select Screen</li> <li>++: Select Item Enter: Select</li> <li>+/-: Change Opt.</li> <li>F1: General Help</li> </ul>
Advanced CPU Flex Ratio Override CPU Flex Ratio Settings Hardware Prefetcher Adjacent Cache Line Prefetch Intel (VMX) Virtualization Technology Active Processor Cores Hyper-Threading BIST	[Disable] 29 [Enabled] [Enabled] [Enabled] [A11] [Enabled] [Disable]	<ul> <li>AP threads Handoff to OS Manner from end of POST</li> <li>++: Select Screen 1↓: Select Item Enter: Select +/-: Change Opt.</li> </ul>

Hyper-Threading[Enabled]after AUX content getsBIST[Disable]reseted.AP threads Idle[MWAIT Loop]nenenenenenenenenenenenenenenenenenene	Aptio Setup Utility Advanced	y – Copyright (C) 2018 Ame	rican Megatrends, Inc.
MonitorMWait[Enabled]++: Select ScreenIntel Trusted[Disable]†4: Select ItemExecution TechnologyEnter: SelectAlias Check Request[Disable]+/-: Change Opt.DPR Memory Size (MB)4F1: General HelpReset AUX Content[no]F2: Previous Values	Active Processor Cores Hyper-Threading BIST AP threads Idle Manner AP threads Handoff Manner AES MachineCheck MonitorMWait Intel Trusted Execution Technology Alias Check Request DPR Memory Size (MB)	[Enabled] [Disable] [MWAIT Loop] [MWAIT Loop] [Enabled] [Enabled] [Disable] [Disable] 4	Txt may not functional after AUX content gets reseted. **: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit

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AB

Feature	Options	Description
SW Guard Extensions	Enabled	
(SGX)	Disabled	Enable/Disable Software Guard Extensions (SGX)
CDU Elso Datia Osseriale	Disabled	
CPU Flex Ratio Override	Enabled	Enable/Disable CPU Flex Ratio Programming
CPU Flex Ratio Settings	29	This value must be between Max Efficiency Ratio (LFM) and Maximum non-turbo ratio set by Hardware (HFM).
Llardwara Drafatahar	Disabled	
Hardware Prefetcher	Enabled	To turn on/off the MLC streamer prefetcher.
Adjacent Cache Line	Disabled	
Prefetch	Enabled	To turn on/off prefetching of adjacent cache lines.
Intel (VMX) Virtualization	Disabled	When enabled, a VMM can utilize the additional hardware
Technology	Enabled	capabilities provided by Vanderpool Technology.
	ALL	
Active Processor Cores	1	Number of cores to enable in each processor package.
	Disabled	Enabled for Windows XP and Linux (OS optimized for
Hyper-Threading	Enabled	Hyper-Threading Technology) and Disabled for other OS. (OS not optimized for Hyper-Threading Technology).

BIST	Disabled Enabled	Enable/Disable BIST (Built-In Self Test) on reset.
	HALT Loop	
AP Threads Idle Manner	MWAIT Loop	AP threads Idle Manner for waiting signal to run.
	RUN Loop	
AP Threads Handoff	HALT Loop	
Manner	MWAIT Loop	AP threads Handoff to OS Manner from end of POST
450	Disabled	
AES	Enabled	Enable/Disable AES (Advanced Encryption Standard)
	Disabled	
MachineCheck	Enabled	Enable/Disable Machine Check
	Disabled	
MonitorMWait	Enabled	Enable/Disable MonitorMWait
Intel Trusted Execution	Disabled	Enables utilization of additional hardware capabilities
Technology	Enabled	provided by Intel <sup>®</sup> Trusted Execution Technology. Changes require a full power cycle to take effect.
	Disabled	Enables Txt Alias Checking capability. Changes require full
Alias Check Request	Enabled	Txt capability before it will take effect. It is a one time only
		change, next reboot will be rest.
DPR Memory Size (MB)	4	Reserve DPR memory size (0-255) MB
Reset AUX Content	Yes	Reset TPM Aux content. Txt may not functional after AUX
	No	content gets reseted.

#### **Power & Performance**

Power & Performance	CPU – Power Management Control Options
CPU – Power Management Control	
	<pre>++: Select Screen  ++: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit</pre>

#### **CPU - Power Management Control**

Aptio Setup Utility Advanced	y – Copyright (C) 2018	American Megatrends, Inc.
CPU – Power Management	Control	Select the performance state that the BIOS
Boot performance mode	[Max Non–Turbo Performance]	will set starting from reset vector.
Intel(R) SpeedStep(tm)	[Disable]	
Race To Halt (RTH)	[Enabled]	
Intel(R) Speed Shift Technology	[Disable]	
C states	[Disable]	
		++: Select Screen
		↑↓: Select Item
		Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit ESC: Exit

Feature	Options	Description
	Max Non-Turbo	Select the performance state that the BIOS will set starting
Boot Performance	Performance	from reset vector.
Mode	Max Battery Turbo	
	Performance	
Intel® SpeedStep™	Disabled	Allows more than two frequency ranges to be supported
inter® speedstep	Enabled	
	Disabled	Enable/Disable Race To Halt feature. RTH will dynamically increase CPU frequency in order to enter pkg C-State
Race To Halt (RTH)	Enabled	faster to reduce overall power. (RTH is controlled through
		MSR 1FC bit 20)
Intel <sup>®</sup> Speed Shift	Enabled	Enable/Disable Intel <sup>®</sup> Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for
Technology	Disabled	hardware-controlled P-states.
Catatas	Enabled	Enable/Disable CPU Power Management. Allows CPU to
C states	Disabled	go to C states when its not 100% utilized.

### **PCH-FW Configuration**

Aptio Setup Utility Advanced	y – Copyright (C) 2018 Ameri	ican Megatrends, Inc.
ME Firmware Version ME Firmware Mode ME Firmware SKU ME File System Integrity Value ME Firmware Status 1 ME Firmware Status 2 NFC Support	Normal Mode Corporate SKU 2 0x90000255	When Disabled ME will be put into ME Temporarily Disabled Mode.
ME State ▶ Firmware Update Configu	[Enabled] µration	<pre>++: Select Screen 1↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>

Feature	Options	Description
ME State	Disabled	When Disabled ME will put into ME Temporarily Disabled
	Enabled	Mode

## Firmware Update Configuration

Aptio Setup Advanced		(ht (C) 2018 Ameri	can Megatrends, Inc.
Me FW Image Re-	Flash [Disable		Enable/Disable Me FW Image Re-Flash function.
			<pre>++: Select Screen 1↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>
Version 2.	18.1263. Copyrigh	(C) 2018 America	n Megatrends, Inc.
Feature	Options		Description
Me FW Image	Disabled		

reature		Description
Me FW Image	Disabled	Enable/Disable Me FW Image Re-Flash function.
Re-Flash	Enable	Enable/Disable Me FW Image Re-Flash function.

## Super IO Configuration

Aptio Setup Utility – Copyright (C) 2018 Advanced	American Megatrends, Inc.
<ul> <li>Super IO Configuration</li> <li>Serial Port 1 Configuration</li> <li>Serial Port 2 Configuration</li> <li>Serial Port 3 Configuration</li> <li>Serial Port 4 Configuration</li> <li>Serial Port 5 Configuration</li> </ul>	Set Parameters of Serial Port 1 (COMA)
	<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>
Version 2.18.1263. Copyright (C) 2018 Am	merican Megatrends, Inc. <mark>84</mark>

## Serial Port 1 Configuration

Aptio Setup Utili Advanced	ty – Copyright (C) 2018	American Megatrends, Inc.
Serial Port 1 Configu	ration	Enable or Disable Serial Port (COM)
Serial Port Device Settings		
COM1 MODE COM1 Termination	[RS232] [Disabled]	
		<pre>++: Select Screen  f↓: Select Item Enter: Select +/-: Change Opt. E1: Caranal Halp</pre>
		F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

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Feature	Options	Description
Carriel Dant	Disabled	Frankla av Disable Saviel David (COM)
Serial Port	Enabled	Enable or Disable Serial Port (COM)
Device Settings	NA	IO = 3F8h; IRQ = 4
	RS232	
COM1 Mode	RS485	COM RS-422/485 Support
	RS422	
COM1 Terreinstien	Disabled	COM DC 422/405 Desciver Territoria
COM1 Termination	Enabled	COM RS-422/485 Receiver Termination

## Serial Port 2 Configuration

Aptio Setup Utilit Advanced	y – Copyright (C) 2018 A	merican Megatrends, Inc.
Serial Port 2 Configuration		Enable or Disable Serial Port (COM)
Serial Port Device Settings		
COM2 MODE COM2 Termination	[RS232] [Disabled]	
		<pre>++: Select Screen f↓: Select Item Enter: Select +/-: Change Opt.</pre>
		F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

Feature	Options	Description
Carriel Dant	Disabled	Freekla er Disekla Seriel Dert (COM)
Serial Port	Enabled	Enable or Disable Serial Port (COM)
Device Settings	NA	IO = 2F8h; IRQ = 3
	RS232	
COM2 Mode	RS485	COM RS-422/485 Support
	RS422	
	Disabled	COM DC 422/405 Descriver Territoria
COM2 Termination	Enabled	COM RS-422/485 Receiver Termination

### Serial Port 3 Configuration

Aptio Setup Utility Advanced	– Copyright (C) 2018 Ameri	can Megatrends, Inc.
Serial Port 3 Configurat	ion	Enable or Disable Serial Port (COM)
Serial Port Device Settings		
		<pre> ++: Select Screen  1↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>

B	4	
_	-	

Feature	Options	Description
Serial Port	Disabled Enabled	Enable or Disable Serial Port (COM)
Device Settings	NA	IO = 3E8h; IRQ = 5

## Serial Port 4 Configuration

Aptio Setup Utili Advanced	ty – Copyright (C) 2018 f	American Megatrends, Inc.
Serial Port 4 Configu	ration	Enable or Disable Serial Port (COM)
Serial Port Device Settings		
COM3 MODE COM3 Termination	[RS232] [Disabled]	
		<pre>→+: Select Screen  ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults</pre>
		F4: Save & Exit ESC: Exit

Feature	Options	Description
Carriel Dant	Disabled	Freeble or Dischle Seriel Part (COM)
Serial Port	Enabled	Enable or Disable Serial Port (COM)
Device Settings	NA	IO = 2E8h; IRQ = 11
	RS232	
COM4 Mode	RS485	COM RS-422/485 Support
	RS422	
COM4 Termination	Disabled	COM DS 422/485 Dessiver Termination
COIVIA Termination	Enabled	COM RS-422/485 Receiver Termination

## Serial Port 5 Configuration

Aptio Setup Utilit Advanced	y – Copyright (C) 2018 (	American Megatrends, Inc.
Serial Port 5 Configuration		Enable or Disable Serial Port (COM)
Serial Port Device Settings		
COM4 MODE COM4 Termination	[RS232] [Disabled]	
		<pre>++: Select Screen  \$ ++: Select Item Enter: Select +/-: Change Opt.</pre>
		F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

Feature	Options	Description
Carriel Dant	Disabled	Freekla er Disekla Seriel Dert (COM)
Serial Port	Enabled	Enable or Disable Serial Port (COM)
Device Settings	NA	IO = 2FOh; IRQ = 7
	RS232	
COM5 Mode	RS485	COM RS-422/485 Support
	RS422	
	Disabled	COM DC 422/405 Descriver Territortion
COM5 Termination	Enabled	COM RS-422/485 Receiver Termination

### **Serial Port 6 Configuration**

Feature	Options	Description
Serial Port	Disabled Enabled	Enable or Disable Serial Port (COM)
Device Settings	NA	IO = 2E0h; IRQ = 10

#### **Hardware Monitor**

Pc Health Status		
	: +13 C : +0.880 V : +1.216 V : +5.003 V : +3.323 V	
VSB3.3V	: +3.328 V	<pre>++: Select Screen f↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>

#### LTE Wi-Fi Selector Setting

Aptio Setup Utilit Advanced	y – Copyright (C) 2018 Amer:	ican Megatrends, Inc.
LTE WiFi Selector Sett	ing	Select which Slot would use
Slot1 Selector Slot2 Selector	(LTE) (LTE)	
		++: Select Screen †↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults
Version 2.18.1263	. Copyright (C) 2018 America	F4: Save & Exit ESC: Exit

Feature	Options	Description
Slot1 Selector	Wi-Fi LTE	Select Which Slot would be used
Slot2 Selector	Wi-Fi LTE	Select Which Slot would be used

Β4

### Status LED Configuration

Aptio Setu Advance		ght (C) 2018 American Megatrends, Inc.
Status LED Con	figuration	Configure Status LED
Status LED	[RED]	
		++: Select Screen †↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2	.18.1263. Copyrigh	t (C) 2018 American Megatrends, Inc.
Footuro	Ontions	Description

Feature	Options	Description
Status LED	Dark Green <mark>Red</mark>	Configuration Status LED

### **Serial Port Console Redirection**

	Console Redirection
COM1	Enable or Disable.
Console Redirection [Enabled]	
Console Redirection Settings	
Legacy Console Redirection	
Legacy Console Redirection Settings	
	Mar Onland Deserve
	++: Select Screen ↑↓: Select Item
	Enter: Select
	+/-: Change Opt.
	F1: General Help
	F2: Previous Values
	F3: Optimized Defaults
	F4: Save & Exit
	ESC: Exit

Feature	Options	Description
COM1 Console	Disabled	Console Redirection Enable or Disable
Redirection	Enabled	Console Redirection Enable of Disable

#### **Console Redirection Settings**

COM1	Emulation: ANSI:	
Console Redirection S	Settings	Extended ASCII char
		set. VT100: ASCII char
Terminal Type	[VT100+]	set. VT100+: Extends
Bits per second	[115200]	VT100 to support color,
Data Bits	[8]	function keys, etc.
Parity	[None]	VT-UTF8: Uses UTF8
Stop Bits	[1]	encoding to map Unicode
Flow Control	[None]	
VT-UTF8 Combo Key	[Enabled]	
Support		↔+: Select Screen
Recorder Mode	[Disabled]	↑↓: Select Item
Resolution 100x31	[Disabled]	Enter: Select
Putty KeyPad	[VT100]	+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit

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Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 ANSI	VT100: ASCII char set VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes ANSI: Extended ASCII char set
Bits per second	9600 19200 38400 57600 115200	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 8	Data Bits
Parity	None Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors.
Stop Bits	1 2	Indicates the end of a serial data packet.
Flow Control	None	Flow Control can prevent data loss from buffer overflow

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	Hardware RTS/CTS		
VT-UTF8 Combo	Disabled	Enables VT-UTF8 Combination Key Support for	
Key Support	Enabled	ANSI/VT100 terminals	
Recorder Mode	Disabled	With this mode enabled, only text will be sent. This is to	
Recorder Mode	Enabled	capture Terminal data.	
Resolution 100x31	Disabled	Enables or disables extended terminal resolution	
Resolution 100x31	Enabled		
	VT100		
	LINUX		
Dutty Koy Dod	XTERM86	Solasts Eurotion Koy and Koy Dad on Dutty	
Putty KeyPad	SCO	Selects FunctionKey and KeyPad on Putty	
	ESCN		
	VT400		

### Legacy Console Redirection Settings

Aptio Setup Utilit Advanced	y – Copyright (C) 2018	American Megatrends, Inc.
Legacy Console Redirec Redirection COM Port Resolution Redirect After POST	[COM1] [80×24]	Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages
		<pre>++: Select Screen  f↓: Select Item Enter: Select</pre>
		+/−: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

- 10	21

Feature	Options	Description
Redirection COM Port	COM1	Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages.
Resolution	<mark>80x24</mark> 80x25	On Legacy OS, the Number of Rows and Columns supported redirection.
Redirection After BIOS Post	<mark>Always Enable</mark> Bootloader	When <b>Bootloader</b> is selected, Legacy Console Redirection is disabled before booting to legacy OS. When <b>Always Enable</b> is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to <b>Always</b> <b>Enable</b> .

### **Intel TXT Information**

Aptio Setup Utili Advanced	ty – Copyright (C) 2018 Amer	rican Megatrends, Inc.
Advanced Intel TXT Information Chipset BiosAcm Chipset Txt Cpu Txt Error Code Class Code Major Code Minor Code	Production Fused Production Fused Supported Supported None None None None	<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help</pre>
		F1: General help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.18.126	3. Copyright (C) 2018 Americ	can Megatrends, Inc. B4

### PCI Subsystem Settings

Aptio Setup Utility – Copyright (C) 2018 Amer: Advanced	ican Megatrends, Inc.
AMI PCI Driver Version : A5.01.16	Globally Enables or Disables 64bit capable
PCI Settings Common for all Devices: Above 4G Decoding [Disabled]	Devices to be Decoded in Above 4G Address
	Space (Only if System
Change Settings of the Following PCI Devices:	Supports 64 bit PCI Decoding).
WARNING: Changing PCI Device(s) settings may have unwanted side effects! System may HANG! PROCEED WITH CAUTION.	
	++: Select Screen
	†∔: Select Item Enter: Select
	+/-: Change Opt.
	F1: General Help
	F2: Previous Values F3: Optimized Defaults
	F4: Save & Exit
	ESC: Exit

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Feature	Options	Description
Above 4G Decoding	Disabled Enabled	Globally Enables or Disables 64bit capable devices to be decoded in above 4G address space (only if System supports 64bit PCI decoding)

### **Network Stack Configuration**

Aptio Setup Advanced		ght (C) 2017 Amer	rican Megatrends, Inc.
Network Stack	[Disable	[k	Enable/Disable UEFI Network Stack ++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.	19.1268. Copyrigh	t (C) 2017 Americ	an Megatrends, Inc. B
Feature	Options		Description

Feature	Options	Description
Network Stack	Disabled Enabled	Enables or disables UEFI Network Stack

### **CSM Configuration**

Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc. Advanced		
Compatibility Support M	odule Configuration	Enable/Disable CSM Support.
CSM Support	[Enabled]	Support.
CSM16 Module Version	07.81	
Option ROM execution		
Network Storage Video Other PCI devices	[Legacy] [Legacy] [Legacy] [Legacy]	<pre> ++: Select Screen  t↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>

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Feature	Options	Description
CSM Support	Disabled Enabled	Enables/Disables CSM Support
Network	Do Not Launch UEFI Legacy	Controls the execution of UEFI and Legacy PXE OpROM
Storage	Do Not Launch UEFI Legacy	Controls the execution of UEFI and Legacy Storage OpROM
Video	Do Not Launch UEFI <mark>Legacy</mark>	Controls the execution of UEFI and Legacy Video OpROM
Other PCI Device	Do Not Launch UEFI <mark>Legacy</mark>	Determines OpROM execution policy for devices other than Network, Storage, or Video

### **NVMe Configuration**

Aptio Setup Utility – Copyright (C) 2018 Ameri Advanced	ican Megatrends, Inc.
NVMe controller and Drive information	
No NVME Device Found	++: Select Screen ↑↓: Select Item
	Enter: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.18.1263. Copyright (C) 2018 America	an Megatrends, Inc. B4

### **USB Configuration**

Aptio Setup Utilit Advanced	y – Copyright (C) 2018 Amer.	ican Megatrends, Inc.
USB Configuration		Enables Legacy USB support. AUTO option
USB Module Version	19	disables legacy support if no USB devices are
USB Controllers: 1 XHCI		connected. DISABLE option will keep USB
USB Devices:		devices available only
2 Drives, 1 Keyb	oard, 3 Hubs	for EFI applications.
	[Enabled]	
USB Mass Storage Driver Support	[Enabled]	↔: Select Screen †↓: Select Item
		Enter: Select
Mass Storage Devices:		+/-: Change Opt.
Generic Ultra	[Auto]	F1: General Help
HS-SD/MMC		F2: Previous Values
SRT USB 1100	[Auto]	F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit

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Feature	Options	Description
Legacy USB Support	Enabled Disabled Auto	<b>Enables</b> Legacy USB support <b>Auto</b> option disables legacy support if no USB devices are connected; <b>Disabled</b> option will keep USB devices available only for EFI applications
USB Mass Storage Driver Support	Disabled Enabled	Enables or disables USB Mass Storage Driver Support

# Chipset

Select the **Chipset** menu item from the BIOS setup screen to enter the "Chipset" setup screen. Users can select any of the items in the left frame of the screen.

Aptio Setup Utility – Copyright (C) 2018 Main Advanced Chipset Security Boot Sav	
▶ System Agent (SA) Configuration ▶ PCH-IO Configuration	System Agent (SA) Parameters
	<pre>++: Select Screen f↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>
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## System Agent (SA) Configuration

Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc. Chipset		
System Agent (SA) Conf.	iguration	Memory Configuration Parameters
SA PCIe Code Version VT–d	2.9.2.0 Supported	
<ul> <li>Memory Configuration VT-d Above 4GB MMIO BIOS assignment</li> </ul>	[Enabled] [Disabled]	
X2APIC Opt Out	[Disabled]	<pre>→+: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>

Feature	Options	Description
VT-d	Disabled Enabled	VT-d capability
Above 4GB MMIO BIOS assignment	Disabled Enabled	Enable/Disable above 4GB MemoryMappedIO BIOS assignment. This is enabled automatically when Aperture Size is set to 2048MB
Z2APIC Opt Out	Disabled Enabled	Enable/Disable X2APIC_OPT_OUT bit

### **Memory Configuration**

emory Configuration		Maximum Memory			Maximum Value of TOLUD
Hemory RC Version Hemory Frequency Hemory Timings (tCL−tRCD−tRP−tRAS)	2.9.2.0 2133 MHz 15-15-15-35	Frequency Selections in Mhz.	Channel 0 Slot 0 Size Number of Ranks Manufacturer Channel 0 Slot 1 Channel 1 Slot 0	Populated & Enabled 16384 MB (DDR4) 2 UnKnown Not Populated / Disabled Not Populated / Disabled	
hannel O Slot O Size Number of Ranks	Populated & Enabled 16384 MB (DDR4)		Channel 1 Slot 1	Not Populated / Disabled	Controller
Manufacturer	2 UnKnown	++: Select Screen	Memory ratio/reference		↔: Select Screen
hannel O Slot 1	Not Populated / Disabled	t∔: Select Item	clock options moved		↑↓: Select Item
hannel 1 Slot O	Not Populated / Disabled	Enter: Select	to		Enter: Select
hannel 1 Slot 1	Not Populated / Disabled	+/-: Change Opt.	Overclock->Memory->Cu		+/-: Change Opt.
		F1: General Help F2: Previous Values	stom Profile menu Maximum Memory		F1: General Help F2: Previous Values
		F3: Optimized Defaults	Frequency		F3: Optimized Defaults
		F4: Save & Exit	Max TOLUD		F4: Save & Exit
		ESC: Exit			ESC: Exit

Feature	Options	Description
Maximum Memory Frequency	Auto 1067~3733	Maximum Memory Frequency Selections in MHz
Max TOLUD	Dynamic 1GB~ 3.5GB	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

### **PCH-IO Configuration**

Aptio Setup Utility – Copyright (C) 2018 A Chipset	merican Megatrends, Inc.
<ul> <li>PCH-IO Configuration</li> <li>PCI Express Configuration</li> <li>SATA And RST Configuration</li> <li>Security Configuration</li> </ul>	PCI Express Configuration settings
Serial IRQ Mode [Continuous] Restore AC Power Loss [Power Off]	<pre></pre>

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Feature	Options	Description
Serial IRQ Mode	Quiet Continuous	Configure Serial IRQ mode
Restore AC Power Loss	Power ON Power OFF	Specify what state to go to when power is re-applied after a power failure (G3 state)

## **PCI Express Configuration**

Aptio Setup Utility – Copyright (C) 2018 Ameri Chipset	can Megatrends, Inc.
PCI Express Configuration	PCI Express Root Port 1 Settings.
▶ PCI Express Root Port 1	
PCI Express Root Port 2	
PCI Express Root Port 3	
PCI Express Root Port 4	
PCI Express Root Port 9	
PCI Express Root Port 10	
	↔: Select Screen
	†∔: Select Item
	Enter: Select
	+/-: Change Opt.
	F1: General Help
	F2: Previous Values
	F3: Optimized Defaults
	F4: Save & Exit
	ESC: Exit
	n Madathanda Taa
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	B4

	ity – Copyright (C) 20: pset	18 American Megatrends, Inc.
PCI Express Root Port 1 ASPM Advanced Error Reporting PCIe Speed Detect Timeout	[Disable]	Control the PCI Express Root Port.
		<pre>++: Select Screen 1↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>
Version 2.18.12	63. Copyright (C) 2018	American Megatrends, Inc. B4

Feature	Options	Description
PCI Express Root Port1	Disabled Enabled	Control the PCI Express Root Port
ASPM	Auto LOsL1 L1 LOs Disabled	Set the ASPM Level: Force all links to 0s State AUTO – BIOS auto configure DISABLE – Disabled ASPM
Advanced Error Reporting	Disabled Enabled	Advanced Error Reporting Enable/Disable
PCIe Speed	Auto Gen1 Gen2 Gen3	Configure PCle Speed
Detect Timeout	0	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.

	ity – Copyright (C) 20 pset	18 American Megatrends, Inc.
PCI Express Root Port 2	[Enabled]	Control the PCI Express Root Port.
ASPM	[Disable]	
Advanced Error Reporting	[Enabled]	
PCIe Speed	[Auto]	
Detect Timeout	0	
		++: Select Screen
		↑↓: Select Item
		Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit

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**B**4

Feature	Options	Description
PCI Express Root Port2	Disabled Enabled	Control the PCI Express Root Port
ASPM	Auto LOsL1 L1 LOs Disabled	Set the ASPM Level: Force L0s - Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disabled ASPM
Advanced Error Reporting	Disabled Enabled	Advanced Error Reporting Enable/Disable
PCIe Speed	Auto Gen1 Gen2 Gen3	Configure PCIe Speed
Detect Timeout	0	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.

	ity – Copyright (C) 20: oset	18 American Megatrends, Inc.
PCI Express Root Port 3	[Enabled]	Control the PCI Express Root Port.
ASPM	[Disable]	
Advanced Error Reporting	[Enabled]	
PCIe Speed	[Auto]	
Detect Timeout	0	
		↔+: Select Screen
		↑↓: Select Item
		Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit

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	s	а	

Feature	Options	Description	
PCI Express Root	Disabled	Control the PCI Express Root Port	
Port3	Enabled	·	
	Auto		
	L0sL1		
ASPM	L1	Set the ASPM Level: Force L0s - Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disabled ASPM	
	LOs		
	Disabled		
Advanced Error	Disabled		
Reporting	Enabled	Advanced Error Reporting Enable/Disable	
	Auto		
PCle Speed Gen1 Gen2 Gen3	Gen1	Configure DCIe Speed	
	Gen2	Configure r Cle Speed	
Detect Timeout	0	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.	

Chipset		an Megatrends, Inc.
PCI Express Root	[Enabled]	Control the PCI Express Root Port.
ASPM	[Disable]	
Advanced Error Reporting	[Enabled]	
PCIe Speed	[Auto]	
Detect Timeout (	0	
		++: Select Screen
		↑↓: Select Item
		Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit

	B4			
Feature	Options	Description		
PCI Express Root Port3	Disabled Enabled	Control the PCI Express Root Port		
ASPM	Auto L0sL1 L1 L0s Disabled	Set the ASPM Level: Force L0s - Force all links to L0s Stat AUTO – BIOS auto configure DISABLE – Disabled ASPM		
Advanced Error Reporting	Disabled Enabled	Advanced Error Reporting Enable/Disable		
PCIe Speed	Auto Gen1 Gen2 Gen3	Configure PCIe Speed		
Detect Timeout	0	The number of milliseconds reference code will wait for line to exit Detect state for enabled ports before assuming the is no device and potentially disabling the port.		

	ity – Copyright (C) 20 pset	18 American Megatrends, Inc.
PCI Express Root Port 9	[Enabled]	Control the PCI Express Root Port.
ASPM	[Disable]	
Advanced Error Reporting	[Enabled]	
PCIe Speed	[Auto]	
Detect Timeout	0	
		→+: Select Screen
		↑↓: Select Item
		Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit

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Feature	Options	Description
PCI Express Root Port3	Disabled Enabled	Control the PCI Express Root Port
ASPM	Auto L0sL1 L1 L0s Disabled	Set the ASPM Level: Force L0s - Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disabled ASPM
Advanced Error Reporting	Disabled Enabled	Advanced Error Reporting Enable/Disable
PCIe Speed	Auto Gen1 Gen2 Gen3	Configure PCIe Speed
Detect Timeout	0	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.

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	ity – Copyright (C) 20 oset	18 American Megatrends, Inc.
PCI Express Root Port 10 ASPM Advanced Error Reporting PCIe Speed	[Disable]	Control the PCI Express Root Port.
Detect Timeout	0	<pre>++: Select Screen 1↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>

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Feature	Options	Description	
PCI Express Root	Disabled		
Port3	Enabled	Control the PCI Express Root Port	
	Auto		
	L0sL1		
ASPM	L1	Set the ASPM Level: Force L0s - Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disabled ASPM	
	LOs	·····	
	Disabled		
Advanced Error	Disabled	Advanced Franz Deservices Frankla (Dissible	
Reporting	Enabled	Advanced Error Reporting Enable/Disable	
	Auto		
PCIe Speed	Gen1	Configure DClo Speed	
	Gen2	Configure PCIe Speed	
	Gen3		
Detect Timeout	0	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.	

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### SATA and RST Configuration

Aptio Setup Utility Chipse	– Copyright (C) 2018 Ameri	can Megatrends, Inc.
SATA Device Type SATA-2 Software Preserve Port 1 Hot Plug Configured as eSATA	<pre>[Enabled] [AHCI] Empty Unknown [Enabled] [Disable] Hot Plug supported [Disable] [Hard Disk Drive] Empty Unknown [Enabled] [Disable] Hot Plug supported</pre>	Enable/Disable SATA Device. ++: Select Screen tl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Hot Plug Configured as eSATA	[Disable]	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive **: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

Feature	Options	Description
SATA Controller(s)	Enabled Disabled	Enable/Disable SATA Device
SATA Mode Selection	AHCI Intel RST	Determines how SATA Controller(s) operate
Port 0/1/2	Disabled Enabled	Enable or Disable SATA Port
Hot Plug	Disabled Enabled	Designates this port as Hot Pluggable
Spin Up Device	Disabled Enabled	If enabled for any of ports Staggered Spin Up with be performed and only the drivees which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	Hard Disk Drive Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive

### **Security Configuration**

Aptio Setup L	Jtility – Copyright (C) 20 Chipset	18 American Megatrends, Inc.
Security Configur	ration	Enable will lock bytes 38h–3Fh in the
RTC Lock	[Enabled]	lower/upper 128-byte
BIOS Lock	[Enabled]	bank of RTC RAM
		<pre>++: Select Screen  f↓: Select Item Enter: Select +/-: Change Opt. F1: General Help</pre>
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit

Feature	Options	Description
RTC Lock	Disabled Enabled	Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM.
BIOS Lock	Disabled Enabled	Enable/Disable the PCH BIOS Lock Enable feature. Required to enabled to ensure SMM protection of flash.

## Security

Select the **Security** menu item from the BIOS setup screen to enter the "Security" setup screen. Users can select any of the items in the left frame of the screen.

Aptio Setup Utility – Copyright (C) 2018 Americ Main Advanced Chipset Security Boot Save & Ex	
Password Description If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup.	Set Administrator Password
If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights. The password length must be	
in the following range:	↔: Select Screen
Minimum length 3	<b>↑↓:</b> Select Item
Maximum length 20	Enter: Select +/-: Change Opt.
Administrator Password	F1: General Help
User Password	F2: Previous Values F3: Optimized Defaults
▶ Secure Boot	F4: Save & Exit ESC: Exit

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Feature	Options
Administrator Password	If ONLY the Administrator's password is set, it only limits access to Setup and is only asked for when entering Setup.
User Password	If ONLY the User's password is set, it serves as a power-on password and must be entered to boot or enter Setup. In Setup, the user will have Administrator rights.

### **Secure Boot**

Aptio Setup Utilit	y – Copyright (C) 2018 Amer. Security	ican Megatrends, Inc.
System Mode Vendor Keys	Setup Not Modified	Secure Boot activated when: Secure Boot is enabled
Secure Boot	[Disable] Not Active	Platform Key(PK) is enrolled, System mode is
Secure Boot Customization ▶ Restore Factory Keys ▶ Reset To Setup Mode	[Custom]	User/Deployed, and CSM is disabled
▶ Key Management		<pre>++: Select Screen  f↓: Select Item Enter: Select +/-: Change Opt.</pre>
		F1: General Help F2: Previous Values F3: Optimized Defaults
		F4: Save & Exit ESC: Exit

Feature	Options	Description
Secure Boot	Disabled Enabled	Secure Boot is activated when Platform Key (PK) is enrolled, System mode is User/Deployed, and CSM function is disabled.
Secure Boot Customization	Standard Custom	Customizable Secure Boot mode: In custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.

### Key Management

Aptio Setup Utility	y <mark>rig</mark> h urity		Ameri	can Megatrends, Inc.
Factory Key Provision • Restore Factory Keys • Reset To Setup Mode • Export Secure Boot varia • Enroll Efi Image	ole]			Provision factory default keys on next re-boot only when System in Setup Mode
Device Guard Ready ▶ Remove 'UEFI CA' from DA ▶ Restore DB defaults Secure Boot variable   S	/ouel	Key Source		→+: Select Screen ↑↓: Select Item
▶ Platform Key(PK)		No Keys	•	Enter: Select
Key Exchange Keys	1000	No Keys		+/-: Change Opt.
<ul> <li>Authorized Signatures</li> </ul>		No Keys		F1: General Help
▶ Forbidden Signatures		No Keys		F2: Previous Values
▶ Authorized TimeStamps		No Keys		F3: Optimized Defaults
▶ OsRecovery Signatures		No Keys		F4: Save & Exit ESC: Exit

Feature	Options	Description
Factory Key Provision	Disabled Enabled	Provision factory default keys on next re-boot only when System in Setup Mode.
Restore Factory Keys	None	Force System to User Mode. Configure NVRAM to contain OEM-defined factory default Secure Boot keys.
Enroll Ffi Image	None	Allows the image to run in Secure Boot mode. Enroll SHA256 hash of the binary into Authorized Signature Database (db)
Restore DB defaults	None	Restore DB variable to factory defaults.

### **Boot Menu**

Select the **Boot** menu item from the BIOS setup screen to enter the "Boot" setup screen. Users can select any of the items in the left frame of the screen.

	y – Copyright (C) 2018 Am et Security Boot Save	
Boot Configuration Setup Prompt Timeout Bootup NumLock State Quiet Boot Boot mode select	<mark>5</mark> [On] [Disabled] [LEGACY]	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
FIXED BOOT ORDER Prior Boot Option #1 Boot Option #2 Boot Option #3 Boot Option #4 • USB Drive BBS Prioriti	[Hard Disk] [USB Device:SRT USB 1100] [CD/DVD] [Network]	<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</pre>

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Feature	Options	Description
Setup Prompt Timeout	5	The number of seconds to wait for setup activation key. 65535 means indefinite waiting.
Bootup NumLock State	ON OFF	Select the keyboard NumLock state
Quiet Boot	Disabled Enabled	Enables or disables Quiet Boot option
Boot mode select	LEGACY UEFI DUAL	Select boot mode for Legacy or UEFI

• Choose boot priority from boot option group

• Choose specifies boot device priority sequence from available Group device

### **Save and Exit Menu**

Select the **Save and Exit** menu item from the BIOS setup screen to enter the setup screen. Users can select any of the items in the left frame of the screen.

	opyright (C) 2018 American Megatrends, Inc. ecurity Boot Save & Exit
Save Options Discard Changes and Exit Save Changes and Reset Default Options Restore Defaults Boot Override SRT USB 1100 Generic Ultra HS-SD/MMC	Exit system setup without saving any changes.
	++: Select Screen †↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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### **Discard Changes and Exit**

Select this option to quit Setup without saving any modifications to the system configuration. The following window will appear after the "Discard Changes and Exit" option is selected. Select "Yes" to Discard changes and Exit Setup.

[ Exit	Without	Saving -
Quit	without	saving?
Yes		NO

### **Save Changes and Reset**

When Users have completed the system configuration changes, select this option to save the changes and reset from BIOS Setup in order for the new system configuration parameters to take effect. The following window will appear after selecting the "Save Changes and Reset" option is selected. Select "Yes" to Save Changes and reset.



### **Restore Defaults**

Restore default values for all setup options. Select "Yes" to load Optimized defaults.



PS: The items under Boot Override were not same with image. It should depend on devices connect on system.

# **APPENDIX A: LED INDICATOR EXPLANATIONS**

### Power / Status / Storage

The status explanations of LED indicators on front panel are as follows:

LED	COLOR	LED ACTION	DESCRIPTION
Dannan	Green	Steady	System is powered ON
Power	OFF	N/A	System is powered OFF
	Green	Steady	System is Active
Chatura	Red	Steady	System Error
Status	OFF	N/A	System is powered OFF
	Note: Status k	oi-color LED con	trolled by GPIO
Chavasa	Amber	Blinking	Storage (HDD/SSD) Active
Storage	OFF	N/A	No Data Access

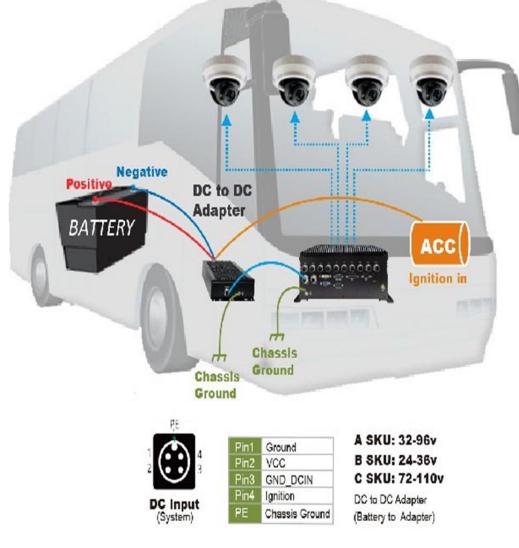
# **APPENDIX B: IGNITION CONTROL SETUP**

### **Connecting the Devices**

The system comes with a controller to ensure that the device is well-shielded against premature failure at the boot or shutdown phase. When installing:

- 1. Make sure both your vehicle and the system are turned off.
- Follow the wiring definition and illustration below to connect the vehicle battery and ignition (ACC) to the in-vehicle system through the 5-pin M12 male connector marked as "DC Input" on the system, through the right pin contact.

In a typical in-vehicle computing solution, this system usually acts as a PSE (Power Sourcing Equipment) to power up connected PoE devices, for which you should ensure a minimum of 48V DC power supply to the system with the use of a **DC to DC Adapter.** 



### DC to DC Converter Description

### Front

M12 K-Code Male

DC Input





PIN		Description	
PIN 1	GND	Primary Ground	
PIN 2	DC_IN	DC Power Input (Isolated)	
PIN 3	GND	Primary Ground	
PIN 4 IGN_IN		Power ON Trigger form car ignition ON	
PIN 5 (PE)	CHASSIS GND	Chassis Ground	
Note: SKU A	.: DC 32~96V		
SKU B: DC 24~36V			
SKU	SKU C: DC 72~110V		

### Rear

### M12 K-Code Female

### DC Output





		Description	
PIN 1	IGN_OUT	Adapter Ignition on Trigger Signal	
PIN 2	MCU_PG	MCU Power_good detect pin (Isolated)	
PIN 3	DC 54V Output	54V Output	
PIN 4	GND	Secondary Ground (S_G for NVR)	
PIN 5 (PE)	CHASSIS GND	Chassis Ground	

Descriptio

### System / NVR Description

M12 K-Code Male

DC Input





	PIN	Description		
PIN 1	GND	Signal Ground		
PIN 2	DC_IN	DC Power Input (from DC converter, 52V)		
PIN 3	MCU_PG	System Power Good Status		
		(without isolated because EMI solution)		
PIN 4	IGN_IN	Ignition on Trigger Form Adapter		
		(Ignition voltage support: 12V or 24V)		
PIN 5 (PE)	CHASSIS GND	Chassis Ground		
Note: DC_in, below 44V without PoE power support				
DC_in, above 45V enable PoE power support				

### Power to System DC IN 54V Cable

DH

M12 H	(-Code Male		M12 K	-Code Female
PIN 1	IGN_IN		PIN 1	GND
PIN 2	MCU_PG		PIN 2	DC_IN
PIN 3	DC_IN		PIN 3	MCU_PG
PIN 4	GND		PIN 4	IGN_IN
PIN 5 (PE)	Chassis GND		PIN 5 (PE)	Chassis GND
	PE 4	Cable	4	PE
2	3		3-	

## Using the Ignition System Manager (ISM)

### **Command Format:**

- 1. Host communication interface: COM#6 (RS-232)
- 2. Support buad rate: 57600/ 8N1
- 3. Communication protocol: ANSI terminal
- **GET VariableName**
- SET VariableName value

MCU Command	Wirte/Read (SET/GET)	VariableName	VariableName value	
	SET	STARTUP_VOLTAGE	0(default)	0mV
Startup Voltage(mV)	GET	STARTUP_VOLTAGE		
Shutdowm	SET	INPUT_VOLTAGE_MIN	8500(default)	8500mV
Voltage(mV)	GET	INPUT_VOLTAGE_MIN		
	SET	POWERON_DELAY	4(default)	4S
PowerOn Delay (Sec)	GET	POWERON_DELAY		
PowerOff Delay (Sec)	SET	SHUTDOWN_DELAY	4(default)	4S
PowerOn Delay (Sec)	GET	SHUTDOWN_DELAY		
Input Voltage	GET	INPUT_VOLTAGE		
Wakeup Dl1	SET	WAKEUP_ENABLE	7(default)	1:DI1 2:Reserved 4: Reserved
Device ID	GET	DEVICE_ID	R6S_N	
Firmware Version	GET	VERSION	0.06B	
Digital Out (LTE on/off)	SET	DIGITAL_OUT	31(default)	
Digial In	GET	DIGITAL_IN		
Ignition	GET	IGNITION		
	SET	DIGITAL_POE	1023( <mark>default</mark> )	0~1023
Digital POE	GET	DIGITAL_POE		
Digital DO	SET	DIGITAL_DO	0(default)	0~255
Digital DI	GET	DIGITAL_DI		
Save flash	SAVE			

#### **Example:**

1. The minimum voltage for startup,

Setting: 6V (6000mV).

Command	Response Message	
SET STARTUP_VOLTAGE 6000.1	OK.1	
GET STARTUP_VOLTAGE1	STARTUP_VOLTAGE = 6000.1	

2. The delay time for POWERON\_DELAY state,...

#### Setting: 4S.

Command	Response Message
SET POWERON_DELAY4.3	OK.1
GET STARTUP_DELAY.1	POWERON_DELAY=4.1

#### Wakeup DI1 Enable,

Setting: DI1 enable (001).

Command	Response Message
SET WAKEUP_ENABLE1.1	OK.1
GET WAKEUP_ENABLE	WAKEUP_ENABLE=1.1

#### 4. Device ID.

Command	Response Message	
GET DEVICE_ID.1	DEVICE_ID=R6S_N.1	]

#### 5. Firmware Version

Command	Response Message	
GET VERSION.1	VERSION=0.6B.1	],

### 6. Write/Read Digital Out state...

#### Setting: LTE module ON/OFF.

Command	Response Message
SET DIGITAL_OUT3.1	OK.1
GET DIGITAL_OUT.1	DIGITAL_OUT=3.1

bit0 = LTE 1(MPCIE) - SIM Control.

1: Power ON.

0: Power OFF.

bit1 = LTE 2(M.2) - SIM Control.

1: Power ON.

0: Power OFF.

bit2 = LTE 3(M.2) - Power Control.

1: Power ON.

0: Power OFF.

bit3 = LTE 4(M.2) - Power Control.

1: Power ON.

0: Power OFF.

bit4 = LTE 5(M.2) - Power Control.

1: Power ON.

0: Power OFF.

#### 7. Read Digital In state.

Command	Response Message	.1
GET DIGITAL_IN a	DIGITAL_IN=3.1	

#### 8. Ignition state (only read).

Command	Response Message	л
GET IGNITION.	IGNITION=0.1	л
	(Orignition OFF / 1: Ignition ON.)	

#### 9. Control the ON/OFF of each PoE port.

Command	Response Message	л
SET DIGITAL_POE1.1	OK.	л
GET DIGITAL_POE	DIGITAL_POE=1.1	.1
POE1/bit0 = 1.		
POE2/bit1 = 2		

POE2/Dit T = 2.1
POE3/bit2 = 4.1
POE4/bit3 = 8.1
POE5/bit4 = 16.
POE6/bit5 = 32.
POE7/bit7 = 64.
POE8/bit7 = 128.
POE9/bit8 = 256.

POE10/bit9 = 512.

To achieve POE1~10 enable, please enter value setting at 1023. ..

.1

10. Write/Read Digital DO state, ..

Setting: DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8.

Command	Response Message a		
SET DIGITAL_DO3.1	OKa a		
GET DIGITAL_DO.1	DIGITAL_DO=3.1		
DO1/bit0 = 1.			
DO2/bit1 = 2.			
DO3/bit2 = 4.			
DO4/bit3 = 8.			
DO5/bit4 = 16.			
DO6/bit5 = 32.			
DO7/bit6 = 64.			
DO8/bit7 = 128			

To achieve DO1~8 enable, please enter value

setting at 255.

#### 12. Save setting.

Command a	Response Message	л
SAVE.1	OK FLASH UPDATED.1	л.

-1

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# **APPENDIX C: TERMS AND CONDITIONS**

### **Warranty Policy**

- 1. All products are under warranty against defects in materials and workmanship for a period of one year from the date of purchase.
- 2. The buyer will bear the return freight charges for goods returned for repair within the warranty period; whereas the manufacturer will bear the after service freight charges for goods returned to the user.
- 3. The buyer will pay for the repair (for replaced components plus service time) and transportation charges (both ways) for items after the expiration of the warranty period.
- 4. If the RMA Service Request Form does not meet the stated requirement as listed on "RMA Service," RMA goods will be returned at customer's expense.
- 5. The following conditions are excluded from this warranty:
  - Improper or inadequate maintenance by the customer
  - Unauthorized modification, misuse, or reversed engineering of the product
  - Operation outside of the environmental specifications for the product.

### **RMA Service**

#### **Requesting an RMA#**

- 1. To obtain an RMA number, simply fill out and fax the "RMA Request Form" to your supplier.
- 2. The customer is required to fill out the problem code as listed. If your problem is not among the codes listed, please write the symptom description in the remarks box.
- 3. Ship the defective unit(s) on freight prepaid terms. Use the original packing materials when possible.
- 4. Mark the RMA# clearly on the box.

Note: Customer is responsible for shipping damage(s) resulting from inadequate/loose packing of the defective unit(s). All RMA# are valid for 30 days only; RMA goods received after the effective RMA# period will be rejected.

### **RMA Service Request Form**

When requesting RMA service, please fill out the following form. Without this form enclosed, your RMA cannot be processed.

RMA No	):	Reasons to Return Testing Purpose	Reasons to Return:  □ Repair(Please include failure details) □ Testing Purpose	
Compa	ny:	Contact Person:		
Phone	No.	Purchased Date:		
Fax No	.:	Applied Date:		
Return	Shipping Addr	ess:		
Dippir Dippir	ng by:    Air Fre rs:	ight □ Sea □ Express 		
Item	Model Name	Serial Number	Configuration	

Item	Problem Code	Failure Status

\*Problem Code: 04: FDC Fail 05: HDC Fail 06: Bad Slot

**Request Party** 

 \*Problem Coue.

 01:D.O.A.

 02: Second Time

 03: Keyboard Controller Fail

 09: Cache RMA Problem

 Cocket Bad

 08: Keyboard Controller Fail 11: Hang Up Software 12: Out Look Damage

13: SCSI 19: DIO 13: SCSI 14: LPT Port 15: PS2 20: Buzzer 21: Shut Down 15: PS2 16: LAN 22: Panel Fail 17: COM Port 23: CRT Fail 18: Watchdog Timer 24: Others (Pls specify)

**Confirmed By Supplier** 

Authorized Signature / Date

#### Authorized Signature / Date

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